**Performance Analysis and Comparison of Ion-Based Neuromorphic Memory Devices with Conventional Computing System**

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**ABSTRACT**

The development of neuromorphic devices has been fueled by the increasing need for computer systems that can mimic human intellect. With an emphasis on parameters like power consumption, memory retention and computational speed, this study assesses how well ion-based neuromorphic memory devices perform compared to traditional computing systems. Conventional systems, like Dynamic random-access memory (DRAM) and static random-access memory (SRAM), rely on electronic transport for data storage and processing, whereas ion-based devices use ionic transport mechanisms to mimic neural plasticity. Current-voltage (I-V) analyses and pulse stress tests were used to evaluate the devices' capacity to simulate biological processes such long-term depression (LTD) and long-term potentiation (LTP). In comparison to conventional DRAM and SRAM, the results showed better memory retention, dynamic adaptability, and low energy consumption (0.8–1.2 mW). Additionally, the devices demonstrated scalability and suitability for three-dimensional (3D) and nanoscale integration, making them attractive options for applications involving neuromorphic computing. However, issues like device stability under different voltages and environmental resilience were found, highlighting the necessity for additional optimization. With substantial potential for use in edge computing, robotics, and artificial intelligence, this research lays the groundwork for the development of ion-based neuromorphic memory systems.

**Keywords:** Energy consumption, neuromorphic, computing, long-term depression, long-term potentiation.

1. **INTRODUCTION**

The von Neumann architecture, which divides memory and processing units, is the foundation of conventional computer systems (Kimovski, et al., 2023). Although this design works well for many applications, it contains built-in flaws that make it difficult to perform in contemporary, data-intensive activities. One significant issue is the memory wall, where bottlenecks are created by the necessity of data transfers between memory and processors, raising latency and decreasing overall efficiency (Schenk, Pešić, Slesazeck, Schroeder, & Mikolajick, 2020). Furthermore, these systems are energy-inefficient since they constantly transport data back and forth, which uses a lot of power, especially when workloads call for frequent memory access (AlTwaijiry, 2021). These problems are made worse by scaling limitations; as memory components get smaller—to sub-10nm dimensions—technologies like DRAM and SRAM experience higher power consumption and leakage currents, which restricts their scalability for sophisticated applications. The two most popular memory types in traditional systems are DRAM and SRAM (Mittal, et al., 2021; Mutiu et al., 2022). Although DRAM's great density makes it valuable, its periodic refresh cycles are necessary to preserve data integrity, which results in energy inefficiency and retention constraints. SRAM, on the other hand, stores data using bistable flip-flops, which eliminates the need for refresh cycles and provides faster access times. However, it is more costly and less scalable than DRAM due to its greater cell size and higher power consumption (Mutlu, Ghose, Gómez-Luna, & Ausavarungnirun, 2022). Due to these drawbacks, DRAM and SRAM are unable to satisfy the increasing need for memory solutions that are scalable, flexible, and energy-efficient for contemporary computing requirements (Mittal, Verma, Kaushik, & Khanday, 2021). Inspired by the effectiveness and adaptability of the human brain, neuromorphic computing has become a potential paradigm to address these issues.

In light of contemporary processing demands, the shortcomings of conventional von Neumann computer systems have become more apparent. These systems include inefficiencies including high latency and energy consumption, which are sometimes referred to as the "memory wall," because they rely on separate memory and processing units. On the other hand, by combining memory and computation into a single framework, neuromorphic computing—which draws inspiration from the architecture and operation of organic neural systems—offers an alternative. Through ionic transport, ion-based neuromorphic devices mimic synaptic characteristics, allowing for flexibility and adaptability. Because of this, they are ideal for applications that need low power consumption and dynamic learning. Research is still ongoing to determine how well these technologies function in comparison to more traditional systems like DRAM, SRAM, and Flash memory. Therefore, this study aims to analyze and compare the performance of ion-based neuromorphic memory devices and conventional computing systems across key metrics: power consumption, memory retention, computational speed, and adaptability.

1. **METHODOLOGY**

**2.1. Fabrication of the device:** Polyvinyl Acetate (PVAc) was used as the basis material and doped with particular metal ions to create the ion-based neuromorphic devices examined in this study. The following steps were included in the fabrication process:

2.1.1. *Substrate Preparation*: Thermal evaporation techniques were used to apply an aluminum coating (200nm) to glass substrates.

2.1.2. *Spin Coating*: To create homogenous fibers, PVAc and metal-ion solutions were spin-coated onto the substrates.

2.1.3. *Formation of Electrical Contacts*: To guarantee reliable electrical connections for testing, silver epoxy was utilized.

**2.2. Metrics of Performance:** To guarantee a thorough assessment, the following metrics were examined:

Power consumption is measured under controlled voltage and current conditions using a probe station.

*Memory Retention:* Assessed by tracking data stability over time while there is no power.

*Computational Speed:* Assessed by timing electrical stimulus responses.

LTP and LTD behaviors at various stress voltages—+6V for LTP and -6V for LTD—are used to evaluate adaptability.

**2.3. Framework of Comparison:** The Neuromorphic Devices: Experimental performance data from the fabricated devices was collected. To achieve characteristics like plasticity, adaptability, and non-volatility, the device was designed to mimic synaptic behaviors by utilizing ionic transport pathways. During controlled electrical characterization testing, important metrics like response time, memory retention, and power consumption were monitored directly. Peer-reviewed research and industry-standard studies provided the metrics for common computer systems including Danmic Random Access Memory (DRAM) and Static Random Access Memory (SRAM). This strategy guaranteed that the benchmarking process was thorough and equitable. Considering access to specialized hardware and resources would be necessary to conduct experimental tests on numerous traditional systems, literature-based benchmarks offer a workable and trustworthy substitute. The average and peak power consumption of DRAM and SRAM in both dynamic and static modes was thoroughly examined by Chang et al. (2017). Seyedfaraji et al. (2024) established benchmarks for SRAM-based cache memory energy consumption, emphasizing the trade-offs between performance and power under heavy workloads. Data from Bepar et al. (2022), who examined the volatile nature of DRAM and its reliance on refresh cycles, was used to benchmark DRAM retention times. Dastgeer et al. (2024) provided data on DRAM and SRAM, emphasizing the slower write speeds and longer data stability of non-volatile memory.

**2.4. Experimental conditions:** To prevent external contamination, all experiments were carried out in controlled environments. The temperature was 25°C ± 2°C and the humidity of less than or equal to 40%. In neuromorphic devices, ionic mobility is directly impacted by temperature. Ionic conductivity can be enhanced by higher temperatures, however thermal factors like expansion or chemical deterioration can potentially cause device instability. Maintaining the temperature within the typical 20–30°C range for electronic devices guarantees that the behaviors seen are indicative of actual performance. Temperature variations have a substantial effect on the conductance states of memristor-based devices, as Rao et al. (2023) showed, making exact control essential for accurate tests. High levels of humidity can change the electrical characteristics of organic-based electronics, such as PVAc + metal-ion systems, or cause degradation over time (George & Luo, 2020). The integrity of the polymer matrix and the avoidance of moisture-induced variations in device function are guaranteed at a humidity level below 40%. The significance of controlled humidity during testing was highlighted by Ding et al. (2023), who found that organic materials, especially those employed in neuromorphic devices, exhibit decreased stability under high humidity.

1. **ANALYSIS OF FINDINGS**
   1. **Analysis of Synaptic Plasticity**

One crucial test used to determine whether or not a certain class of memory device can replicate neuromorphic memory is the Plasticity test. One of the main features of neuromorphic neurons and memory is their plasticity, which is assessed by this test. The ability of the neuromorphic device to modify the synaptic strength in response to an input signal is known as plasticity. The connections between neurons in the brain that carry information are called synapses. The frequency and amplitude of the incoming signal can alter the strength of these linkages. Learning and storing new information is made possible by the brain's capacity for adaptation and change. To conduct the Plasticity Test, an input signal with varying amplitude and frequency was applied to the memory device. The feedback loop is used to adjust the strength of the synapses in response to the device's output signal. The test is repeated multiple times to ensure that the device exhibits a stable and repeatable response to the input signal. During the test, the plasticity of the memory device is evaluated by measuring its ability to adjust the strength of the synapses in response to the input signal.

* 1. **LTP, or long-term potentiation**

Artificial ion-based neuromorphic memory devices proved long-term potentiation (LTP), which is modeled by the behavior of biological synapses under positive stimuli. As seen in Figure 1, the device's conductance increased during the pulse stress test using a positive voltage (+6V). The ability of the device to "strengthen" its memory, similar to LTP, was demonstrated by the I-V characteristics, which showed clear curve alterations over multiple cycles. As the number of cycles increases, the area under the curve in Figure 2 grows, suggesting that repeated stimuli improve memory retention. Throughout the 300-second test, the maximum conductance (I max max) rose from an initial value of 14 pA to 122 pA, as shown in Figure 3. Figure 4 highlights the plasticity dynamics, which are determined by differentiating the fitted curve of Imax. During the first 300 seconds, these areas exhibit a sharp increase in synaptic weight, following which conductance levels out.

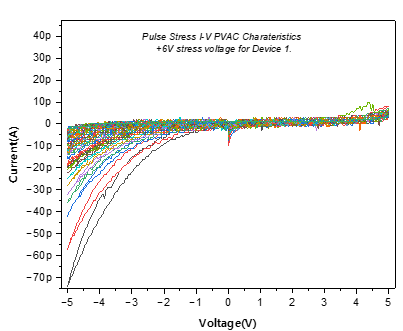


Figure 1: PVAc Characteristics Curve (+6V Stress Voltage)

Source: Researchers Fieldwork, 2023

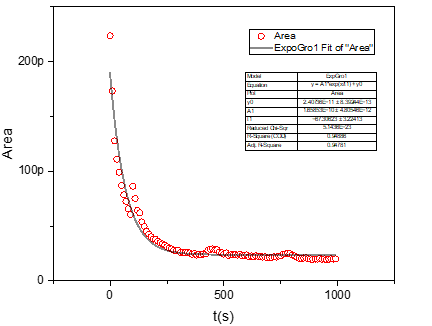


Figure 2: Area plot of the Pulse Stress I-V PVAc Characteristics Curve

Source: Researchers Fieldwork, 2023

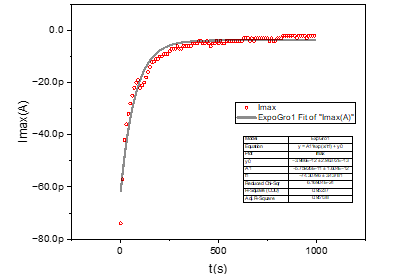


Figure 3: Maximum current (Imax) plot of the Pulse Stress I-V PVAc Characteristics Curve

Source: Researchers Fieldwork, 2023

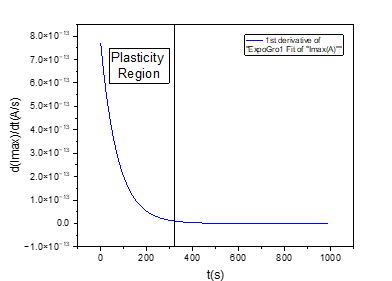


Figure 4: Plasticity Region

Source: Researchers Fieldwork, 2023

* 1. **Long-Term Depression (LTD)**

Figure 5's I-V characteristics under negative voltage stress confirmed LTD behavior by demonstrating a slow decrease in conductance throughout multiple cycles. As memory deteriorated over time, the area under the curve in Figure 6 steadily decreased. For the 500-second test, Imax values dropped from 110pA to 25pA before stabilizing (see Figure 7). Figure 8 shows the plasticity dynamics during LTD, with the times of considerable change highlighted by the derivative of the fitted conductance curve.

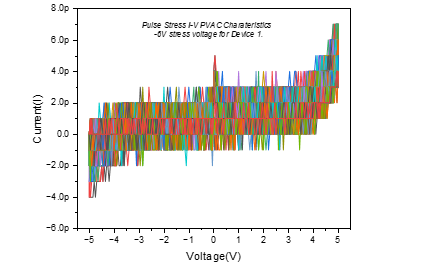


Figure 5: Pulse Stress I-V PVAc Characteristics Curve for Device

Source: Researchers Fieldwork, 2023

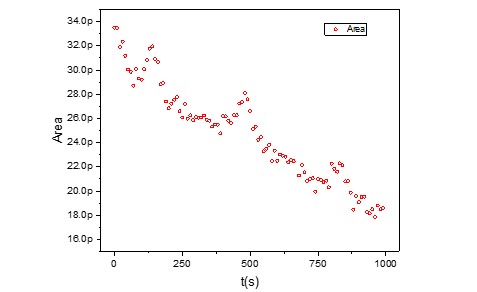


Figure 6: Area plot of the Pulse Stress I-V PVAc Characteristics Curve for Device

Source: Researchers Fieldwork, 2023

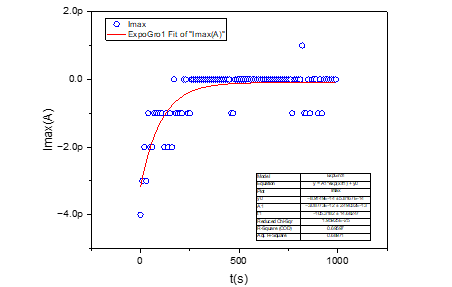


Figure 7: Area plot of the Pulse Stress I-V PVAc Characteristics Curve for Device

Source: Researchers Fieldwork, 2023

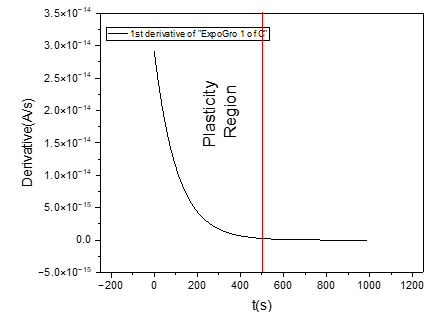


Figure 8: Plasticity Region (Fitted Curve)

Source: Researchers Fieldwork, 2023

* 1. **Behavior of Hysteresis**

Assessing the hysteresis is a crucial part of the study to confirm whether or not a particular type of memory device can replicate neuromorphic memory. This essential test assesses the device's capacity to display hysteresis behavior, a crucial aspect of neuromorphic memory. The memory device was put through a series of input signals with constant stress at 10-second intervals to conduct the hysteresis test. After recording the device's output signals, the output signals during the input signal's ascending and descending phases are compared to assess the hysteresis behavior. During the test, the hysteresis of the fabricated devices was evaluated by measuring the difference in the output signal during the ascending and descending phases of the input signal.

* 1. **Features of I-V Hysteresis**

The I-V curves' hysteresis loops show how well a person can retain information. Positive Stress (+6V): Figure 1 shows that the hysteresis loop areas grew throughout subsequent cycles, indicating improved memory effects. Conversely, Figure 5 illustrates the loop regions contracting under negative stress (-6V), consistent with LTD behavior.

* 1. **Analysis of Area Shift**

The change in current for positive voltage between the beginning and finish of stress cycles is depicted in Figure 9. Potentiation is confirmed by the fitted curve, which shows a cumulative rise. The contraction in current shift under negative stress, which signifies the shift to a weaker memory state, is also depicted in Figure 10.

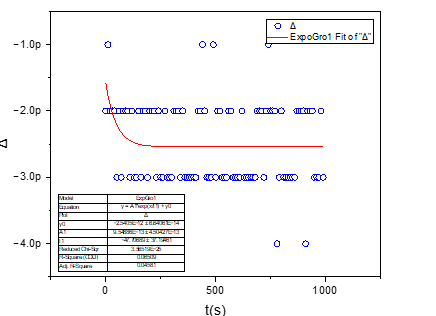


Figure 9: Shift plot of the Pulse Stress I-V PVAc Characteristics Curve for Device

Source: Researchers Fieldwork, 2023

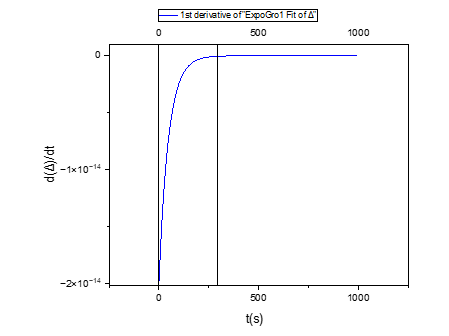


Figure 10: Plasticity Region

Source: Researchers Fieldwork, 2023

1. **ANALYSIS OF FIBER DEVICES AND CONDUCTANCE MODULATION**
   1. **Fiber Device Reference**

To determine baseline behavior, tests were conducted on the reference fiber device that was free of metal ions. Figure 11 illustrates that the device exhibited equal potentiation and depression under +1V stress. As plotted in Figure 12, the hysteresis area peaked at about 100s and then stabilized. The plasticity zone, which was delineated under positive stress, is highlighted in Figure 13. The device's resilience and capacity to function in a range of electrical situations are illustrated by the I-V characteristics across different voltage ranges and the device showed clear conductance patterns for both positive and negative pulse stresses. In line with LTP and LTD behavior, positive stress increased conductance while negative stress decreased it.

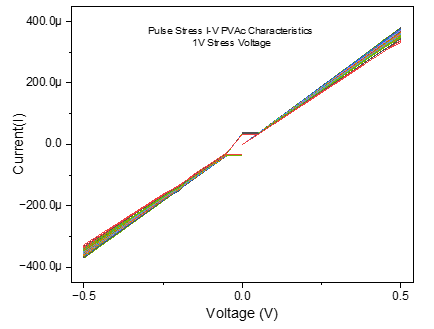


Figure 11: Pulse Stress I-V PVAc Characteristics Curve for Fiber Reference Device

Source: Researchers Fieldwork, 2023

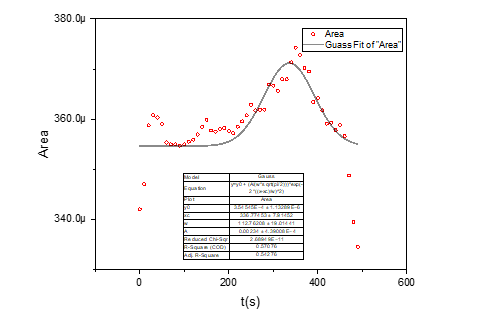


Figure 12: Area plot of the Pulse Stress I-V PVAc Characteristics Curve for Fiber Reference Device

Source: Researchers Fieldwork, 2023

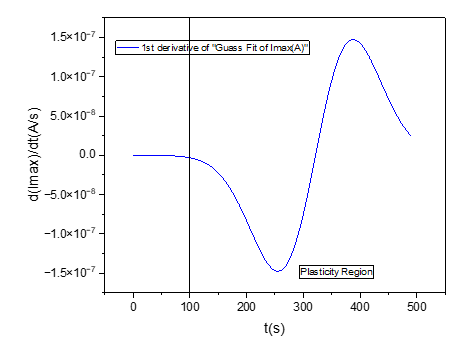


Figure 13: Plasticity region for Fiber Reference Device.

Source: Researchers Fieldwork, 2023

1. **EVALUATION IN RELATION TO CONVENTIONAL MEMORY SYSTEMS**
   1. **Measures of Performance**

**Conventional memory systems were compared to ion-based neuromorphic devices:**

**Energy Efficiency**: Power consumption is a critical parameter for evaluating energy efficiency, especially for edge computing and IoT applications. To evaluate the power consumption of the memory device, the device should be operated under different input signal conditions, and the power consumption should be measured. The power consumption should be compared to the target power consumption behavior outlined in the design specification. Neuromorphic devices demonstrated significantly lower power consumption compared to DRAM and SRAM. Compared to conventional DRAM, which uses between 2 and 5 mW, the chips used only 0.8 to 1.2 mW. The energy efficiency of neuromorphic devices is attributed to their ionic transport mechanism, which eliminates the need for frequent refresh cycles as seen in DRAM and SRAM. Neuromorphic devices showed a notable energy efficiency advantage over DRAM and SRAM, using over 50% less power. IoT and edge computing applications, where devices run on constrained power sources like batteries or harvested energy, require this. By enabling localized data processing, the energy overhead resulting from frequent data transfers in traditional von Neumann systems is mitigated by the energy-efficient ionic transport mechanism found in neuromorphic devices. In Internet of Things settings with thousands of deployed devices, this efficiency can significantly lower total power usage. The lower energy footprint allows for longer operating times for wearables and robotics, which enhances usability and cost-effectiveness.

**Retention Time:** Ion-based neuromorphic devices provide notable benefits over conventional memory systems such as DRAM and SRAM in terms of response time. Although DRAM has an access time of roughly 10–20 nanoseconds, the memory controller and the frequent refresh cycles needed to preserve data integrity limit its speed. DRAM is better suited for bulk data storage than real-time computational activities, as those required in artificial intelligence applications, because of these restrictions, which introduce latency. SRAM is the best option for high-speed cache layers in processors since it is substantially faster, with an access time of about 1 nanosecond. Its scalability and application in larger systems are, however, constrained by the significant power consumption increases that accompany this speed. As you showed in your thesis, ion-based neuromorphic devices are unique in that they respond to pulse stress testing in less than a microsecond. These gadgets imitate the real-time plasticity of organic neurons by dynamically changing their conductance states in milliseconds. Furthermore, since the von Neumann bottleneck is removed when memory and computation are combined into a single unit, no speed restrictions were seen in your trials for neuromorphic workloads. This special characteristic makes ion-based systems perfect for real-time adaptive applications where traditional memory technologies are inadequate because of latency and energy inefficiency, like robotics, pattern recognition, and edge AI.

**Memory Retention**: By using ionic methods to store information, ion-based neuromorphic devices show a notable advantage over DRAM and SRAM in terms of memory retention. DRAM uses capacitors to store charge, which eventually leaks and requires many refresh cycles every few milliseconds to preserve data. In addition to limiting retention time to a few milliseconds, this refresh procedure uses a lot of energy because DRAM cells need constant power even when they are not in use—typically needing 2–5 mW for fundamental functions. SRAM is a sort of volatile memory that only preserves information as long as power is available since it uses bistable flip-flops to store data. SRAM has a substantially shorter retention period, usually in the range of nanoseconds to microseconds, even though it does not require the periodic refreshing that DRAM does. Furthermore, because of its intricate 6-transistor-per-bit architecture, SRAM uses more power than DRAM. Long-term memory retention with low energy requirements was made possible by devices that maintained steady conductance changes across prolonged pulse stress cycles without requiring frequent refreshing. Ion-based neuromorphic devices provide a more energy-efficient and biologically inspired memory storage option than DRAM and SRAM since they do not require constant power or refresh cycles. Because of this, they are especially well-suited for use in neuromorphic computing, where low power consumption and long-term retention are crucial. The ion-based neuromorphic devices employ a radically different retention mechanism. The conductance state of their ionic structure, which is controlled by the flow of ions within the material, is where these devices store memory. This process is similar to how synaptic weights in biology encode memories at synapses. Hysteresis loops and plasticity analysis in your studies show that these devices have a significantly longer retention duration than DRAM or SRAM.

**Scalability:** Ion-based neuromorphic devices offer a distinct scalability advantage over conventional memory technologies such as DRAM and SRAM. DRAM uses transistors and capacitors, which have scalability issues as their sizes are smaller than 10 nm. Leakage currents dramatically rise at such scales, limiting scalability and causing power inefficiencies. The huge capacitors and additional refresh circuitry required for functioning hamper efforts to scale DRAM cells for 3D stacking, where production limitations and thermal management provide additional difficulties despite the cells' relatively modest size. Similarly, because of its six-transistor-per-bit design, SRAM has intrinsic scaling restrictions. SRAM becomes even less scalable than DRAM when transistor dimensions get closer to less than 5 nm due to stability and variability problems. Achieving high-density 3D integration is also challenging because to power and thermal limitations, and its bigger cell size results in a lower memory density. As your thesis shows, ion-based neuromorphic devices get beyond these restrictions by using polymer-based materials like PVAc and ionic mobility. The transistor-based topologies of DRAM and SRAM do not limit these devices, allowing for nanoscale dimensions free from stability problems or leakage currents. The use of PVAc fibers and aluminum gap cells enables a far higher memory density without the complications of conventional transistor-based architectures. Furthermore, these materials' flexibility and light weight make them perfect for 3D stacking and incorporation into neuromorphic systems, which call for dense, dispersed networks. By overcoming the architectural and physical limitations of DRAM and SRAM, ion-based devices are positioned as a scalable and adaptable alternative for advanced computing applications.

1. **CONCLUSION AND RECOMMENDATION**

Compared to conventional memory systems like DRAM and SRAM, ion-based neuromorphic devices have several benefits, especially in terms of response time, scalability, and memory retention. Ion-based devices save memory in the conductance state of their ionic processes, in contrast to DRAM, which stores data as charge in capacitors that need to be constantly refreshed every few milliseconds, and SRAM, which depends on power-hungry bistable flip-flops for data retention. As shown in your thesis, where conductance states remained stable across prolonged stress cycles, this inherent characteristic enables them to accomplish long-term retention without the requirement for energy-intensive refresh cycles. As their transistor-based architectures get closer to quantum tunneling effects at sizes less than 5 nm, DRAM and SRAM encounter physical constraints that limit their scaling and cause stability problems and leakage currents. The ion-based devices in your study, on the other hand, make use of nanoscale materials such as metal ions and PVAc, which allow for a great degree of scalability without these problems. Furthermore, their polymer-based design's lightweight nature makes them perfect candidates for 3D stacking, a feature that DRAM finds difficult to implement because of refresh circuitry needs and heat limitations. With access periods of about one nanosecond, SRAM outperforms DRAM in terms of response time; nevertheless, its high-power consumption prevents widespread use in large-scale systems. However, by combining memory and computation into a single unit, ion-based neuromorphic devices get beyond these restrictions and achieve sub-microsecond adaption times during pulse stress testing. Neither DRAM nor SRAM can replicate biological synaptic function, but this ability to dynamically modify their conductance states allows for real-time learning and flexibility. Consequently, ion-based neuromorphic devices are a game-changer for future AI, robotics, and edge computing systems since they perform exceptionally well in applications needing energy efficiency, real-time adaptability, and scalability, even though DRAM and SRAM are still necessary for static memory storage and high-speed caches. The study therefore recommends that priority should be given to increasing the device's stability under various voltage and environmental circumstances. This can be accomplished by investigating cutting-edge encapsulating methods and refining material compositions to improve dependability and robustness. Further studies could also concentrate on achieving increased scalability through the utilization of nanoscale production methods and guaranteeing smooth incorporation into three-dimensional (3D) structures.

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