**Enhanced Three-Stage Comparator Design for High Speed and Reduced Kickback Noise**

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**ABSTRACT:** This paper introduces a novel three-stage comparator and an enhanced variation designed to boost speed and minimize kickback noise. In contrast to conventional two-stage comparators, the proposed three-stage design incorporates an additional amplification stage, which improves voltage gain and enhances operational speed. Unlike the traditional two-stage comparator, which typically employs a pMOS input pair in the regeneration stage, the three-stage design allows the use of nMOS input pairs in both the regeneration and amplification stages, contributing further to increased speed.To mitigate kickback noise, the modified version of the three-stage comparator features a CMOS input pair in the amplification stage. This configuration effectively cancels nMOS-induced kickback with pMOS kickback, significantly reducing overall noise. As an essential component in many analog-to-digital converters (ADCs), comparators play a critical role in defining the performance of high-speed, high-resolution SAR ADCs. Given these challenges, designing a high-performance comparator is crucial. The proposed three-stage comparator, with its additional amplification stage, achieves greater voltage gain and speed compared to traditional two-stage counterparts. Furthermore, the integration of nMOS input pairs in both key stages enhances speed, while the adoption of a CMOS input pair in theamplification stage of the modified version efficiently minimizes kickback noise.

***KEYWORDS:*** *Comparator, high speed, low kickback, Analog-to-Digital Converters (ADCs), Complementary Metal–Oxide–Semiconductor (CMOS).*

# I.INTRODUCTION

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high- speed, low power comparators with small chip area. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [16]. Hence, designing high- speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs.

The comparator circuit is one of the important building blocks in an analog-to- digital converter which converts one form of signal to another in the operation of RF communications, radio frequency identification (RFID), wireless sensor network (WSN), voltage regulations, brown-out detections, digital signal processing (DSP) [11], high speed processors, and microprocessors. This circuit compares the levels of two analog

input signals and depending on the difference in levels of two signals, the digital output signal can be obtained. In other words, it can be defined that it is a device that compares two currents or two voltages and outputs of a digital signal shows the one which is larger. Currently, researchers are trying to develop the comparator circuits which are faster and have small area with small power consumption [12].

With the rapid development of consumer, automotive and communication electronics the ADC faces increased challenges by power constraints, high speed and low noise. Therefore, as the fundamental building of ADCs the characteristics of comparators determine directly the performance of ADCs. However, comparator suffers from the disturbance of the input signal source due to kickback noise and DC static offset. Hence, the comparator is based on a regenerative latch with two inverters. In the reset phase, both inverters are shorted by the switch. In the regeneration phase the switch opens and the positive feedback regenerates the outputs to supply rail voltages, respectively. But the large variation of output voltages is coupled by the gate-drain capacitance of the input transistors back to the input nodes. Thus, the injected current through the coupled parasitic capacitor produces a kickback noise over the input impedance. This kickback noise can disturb the input signal and leads to errors.

In addition to the differential kickback noise caused by the outputs of the comparator, the clocked input generates also the common mode kickback noise. Especially when the signal source has asymmetric impedance, the common mode kickback noise becomes even worse. In ADCs [20], where the comparators are connected in parallel, the kickback noise can considerably disturb the input signal and limit the performance of ADCs. Therefore, a novel dynamic latched

comparator using common source input transistors and a decoupling mechanism for reducing the common-mode as well as differential kickback noise is presented in this paper.

With the ongoing trend of moving from narrowband to wideband wireless communications, high-speed ADCs are continuing to be a topic of interest. For example, in wideband software defined radio (SDR) receivers with direct RF sampling [17] most analog front-end circuits are replaced by an ADC with a sampling rate of up to several giga- samples per second. The design of high- speed ADCs having low power consumption is challenging but essential for portable applications. Using a single flash ADC can be a solution [19], but due to the large number of comparators, this choice leads to relatively high power consumption especially for medium to high resolutions. Alternatives to flash ADC for high-speed medium-resolution with low-power operation are hybrid and time-interleaved (TI) ADCs [13]. For low resolution and high speed, flash ADCs are power efficient, while SAR ADCs are power efficient for higher resolutions with lower speeds. Considering these features, we constructed a hybrid ADC with a low- resolution flash ADC as the first stage and four low-power TI SAR ADCs in the second stage to achieve high-speed low- power operation.

Many techniques, such as supply boosting methods techniques employing body- driven transistors, current-mode design and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low- voltage design challenges. Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS

technologies. Body-driven technique adopted by Blalock, removes the threshold voltage requirement such that body driven metal–oxide–semiconductor field effect transistors (MOSFET) operates as a depletion-type device. Based on this approach, in, a 1-bit quantizer for modulators is proposed. Despite the advantages, the body driven transistor suffers from smaller transconductance (equal to *gmb* of the transistor) compared to its gate-driven counterpart while special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration.

The rest of the paper is organized as follows: Section II introduces the Literature survey, Section III explains A Three-Stage Comparator And ITS Modified Version With Fast Speed And Llow KICKBACK. Section IV includes the experimental result analysis and finally paper concludes with Section V.

# LITERATURE SURVEY

H. S. Bindra, C. E. Lokin, D. Schinkel, A.-

J. Annema, and B. Nauta, et al.,[7] A 1.2- V Dynamic Bias Latch-Type Comparator in 65-nm CMOS With 0.4-mV Input Noise. A latch-type comparator with a dynamic bias pre-amplifier is implemented in a 65-nm CMOS process. The dynamic bias with a tail capacitor is simple to implement and ensures that the pre- amplifier output nodes are only partially discharged to reduce the energy consumption. The comparator is analyzed and compared to its prior art in terms of energy consumption and input referred noise voltage. First-order equations are presented that show how to optimize the pre-amplifier for low noise and high gain. Both the dynamic bias comparator and the prior art are implemented on the same die and measurements show that the dynamic bias can reduce the average energy consumption by about a factor 2.5 for the same input-equivalent noise at an input

common-mode level of half the supply voltage.

Y. T. Wang et al.,[21] presents An 8-bit 150-MHz CMOS A/D converter. This paper describes an 8-bit 5-stage pipelined and interleaved analog-to-digital converter that performs analog processing only by means of open-loop circuits such as differential pairs and source followers to achieve a high conversion rate. The concept of sliding interpolation is proposed to obviate the need for a large number of comparators or interstage digital-to-analog converters and residue amplifiers. The pipelining scheme incorporates distributed sampling between the stages so as to relax the linearity-speed tradeoffs in the sample-and-hold circuits, A clock edge reassignment technique is also introduced that suppresses timing mismatches in interleaved systems, and a punctured interpolation method is proposed that reduces the integral nonlinearity error with negligible speed or power penalty. Fabricated in a 0.6-/spl mu/m CMOS technology, the converter achieves differential and integral nonlinearities of 0.62 and 1.24 LSB, respectively, and a signal-to- (noise+distortion) ratio of 43.7 dB at a sampling rate of 150 MHz.

S. Babayan-Mashhadi and R. Lotfi et al.,[14] Analysis and Design of a Low- Voltage Low-Power Double-Tail Comparator. The need for ultra low-power, area efficient, and high speed analog-to- digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is

proposed, where the circuit of a conventional double-tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18- μm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced.

A. Khorami and M. Sharifkhani et al.,[8] A explain Low-Power High-Speed Comparator for Precise Applications. A low-power comparator is presented. pMOS transistors are used at the input of the preamplifier of the comparator as well as the latch stage. Both stages are controlled by a special local clock generator. At the evaluation phase, the latch is activated with a delay to achieve enough preamplification gain and avoid excess power consumption. Meanwhile, small cross-coupled transistors increase the preamplifier gain and decrease the input common mode of the latch to strongly turn on the pMOS transistors (at the latch input) and reduce the delay. Unlike the conventional comparator, the proposed structure let us set the optimum delay for preamplification and avoid excess power consumption. The speed and the power benefits of the comparator were verified using solid analytical derivations, process– VDD–temperature corners, and Monte Carlo simulations along with silicon measurements in 0.18 *μ*m .

J. Lu and J. Holleman et al., [15] describe A Low-Power High-Precision Comparator With Time-Domain Bulk-Tuned Offset Cancellation. A novel time-domain bulk- tuned offset cancellation technique is applied to a low-power high-precision dynamic comparator to reduce its input- referred offset with minimal additional

power consumption and delay. The design has been fabricated in a commercially available 0.5-μm process. Measurement results of 10 circuits show a reduction of offset standard deviation from 5.415 mV to 50.57 μV, improved by a factor of

107.1. The offset cancellation scheme does not introduce observable offset or noise, and can achieve fast and robust convergence with a wide range of common mode input. Operating at a supply of 5 V and clock frequency of 200 kHz, the comparator together with the OC circuitry consumes 4.65 μW of power, or 23 pJ of energy per comparison.

M. Shim et al., [9] presents An Energy- Scalable Oscillator Collapse-Based Comparator With Application in a 74.1 dB SNDR and 20 kS/s 15 b SAR ADC. Minimizing power consumption, which can be obtained by reducing feature size, can affect the overall performance. In order to reduce the power dissipation and achieve high speed, the designed circuit at low supply voltage must be operable and also the components should be compact. Therefore, any improved performance in designed comparator, which plays a key role, can take the whole system performance forward and overall successful implementation of a data converter system is achieved. This is the crucial part of the design. Designing high- speed comparators with high-resolution are challenging as they can suffer from low supply voltages.

B. Goll and H. Zimmermann, et al.,[18] In many attempts for achieving high-speed comparators with low voltage supply have been presented. In it is shown that threshold voltages of the devices have not been scaled down by the same factor and reducing the supply voltages can cause the limited range of input common mode voltage. Also, undershoots and overshoots can damage conventional static comparators and cause dissipation of large static power together with speed reduction.

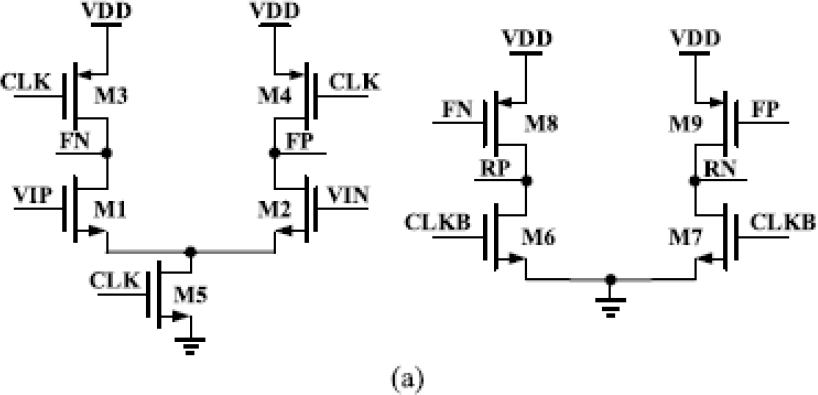
The transfer function for the ideal comparator indicates that a comparator compares the value of input voltage and reference Vref. After comparison is done, it produces logic output value which depends on whether the input voltage is larger or smaller than the reference level. In this paper, input and output offset cancelling topologies are investigated for designing high-speed and high-resolution comparator as Input Offset Cancellation (IOC) is preferable for high-resolution and Output Offset Cancellation (OOC) is preferable for very high-speed comparator applications.

# A THREE-STAGE COMPARATOR AND ITS MODIFIED VERSION WITH FAST SPEED AND

**LOW KICKBACK**

In this paper, presents A Three-Stage Comparator and ITS Modified Version With Fast Speed And Low KICKBACK. Fig.1 shows the three-stage comparator in this work. The three stages are connected one after another. Compared with the Miyahara’s comparator, the major difference is that one extra preamplifier (the second stage) is added. This extra preamplifier acts as an inverter, and makes the latch stage able to use nMOS input pair M11–12 instead of pMOS input pair, which leads to increased speed. The extra preamplifier also provides voltage gain, thus improving the regeneration speed and suppressing the input referred offset and noise. To this end, this brief presents a three-stage comparator. By adding an extra preamplifier stage, the nMOS input pairs can be used for both the latch-stage and the first-stage preamplifier, thus improving the regeneration speed. Besides, these input pairs work in the saturation region at the beginning of comparison, thus ensuring a small input referred noise. The extra stage of preamplifier also provides voltage gain, which helps further increase the regeneration speed and suppress the input referred offset and noise. Compared to the prior three-stage comparator of, the three-

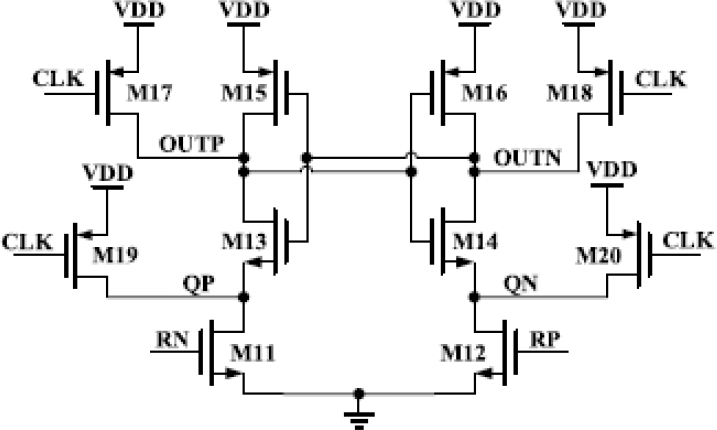
stage comparator in this work has a faster speed and a lower input referred noise. By using a CMOS input pair at the first-stage preamplifier, the kickback noise is greatly reduced. An extra path is also added in the latch stage to further increase the regeneration speed and suppress the input referred offset and noise. Implemented in the same 130-nm process, the three-stage comparator in this work increases the speed compared to the conventional two- stage comparators, while the proposed modified version improves the speed and decreases the kickback noise by ten times.



**Fig. 1: Original first two stages (preamplifiers)**

The extra preamplifier also provides voltage gain, thus improving the regeneration speed and suppressing the input referred offset and noise. Although the extra preamplifier helps increase the speed, this extra stage itself incurs extra delay, because the amplified signal has to go through two stages, rather than one stage, before arriving at the latch stage. Thus, it is necessary to discuss whether this extra delay overwhelms the benefit it brings about. As can be seen in Fig.1, after the first-stage amplification, its outputs FP and FN fall to GND. This makes the second-stage input pair M8–9 have a large gate–source voltage equal to *V*DD. As a result, the current on M8–9 is large enough for quickly pulling up RP and RN. This

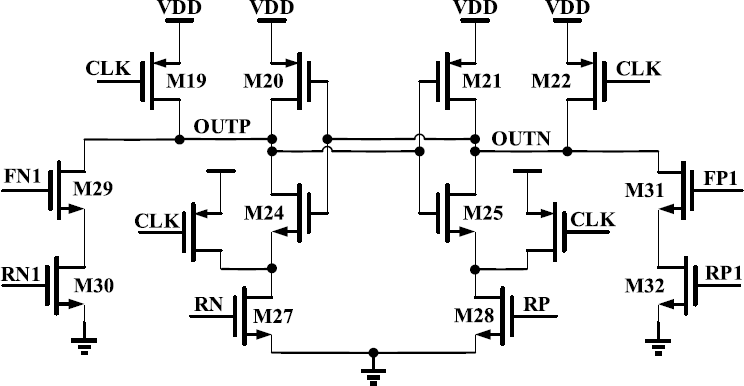
means that the extra delay incurred by the second stage is small (about 20 ps in post- layout simulation) compared to the large delay of the latch stage (about 200 ps in post-layout simulation). This makes sense because the second stage is actually a dynamic inverter which does not incur much delay. Furthermore, compared to the first-stage output load in the Miyahara’s comparator (M6–7 and M12–15 in Fig. 1), the first-stage output load in the three- stage comparator is only M8–9 in Fig.1. The output load is reduced by several times, improving the amplification speed.



**Fig. 2: Extra first two stages (preamplifiers) with PMOS**

Compared to the three-stage comparator in, the three-stage comparator in this work also has several advantages. First, the gate of M6–7 in Fig. 2 is connected to CLKB, rather than to the first-stage output. This reduces the parasitic capacitance at the first-stage output. Second, the gate of M17–20 is connected to CLK, rather than to the second-stage output. This reduces the parasitic capacitance at the second- stage output. Third, the clocked cascade NMOS on top of M1–2 is deleted. This reduces the parasitic capacitance in the first stage. More importantly, it helps ensure that the drain of M1–2 is at *V*DD at the beginning of comparison. This is important, because the saturation region of input pair helps reduce the input referred

noise. This reduces the parasitic capacitance at the second-stage output. Third, the clocked cascode nMOS on top of M1–2 is deleted. This reduces the parasitic capacitance in the first stage. More importantly, it helps ensure that the drain of M1–2 is at *V*DD at the beginning of comparison. This is important, because the saturation region of input pair helps reduce the input referred noise. Overall, post-layout simulated results show that the input referred noise is reduced due to the guaranteed saturation region of input pair, and the speed is increased due to the less parasitic capacitances.



**Fig. 3: Latch Stage**

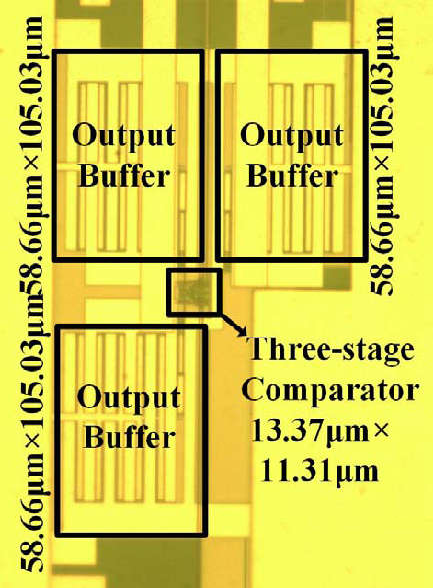
In order to reduce the kickback noise and further improve the speed, this brief proposes a modified version of three-stage comparator. This generates a differential voltage at OUTP and OUTN, which helps speedup the regeneration phase afterward and suppress the comparator input referred offset and noise. After FP1 and FN1 fall to GND, the extra paths are turned off again to prevent the static current. Overall, the modified version of three-stage comparator has the advantages of faster speed, lower input referred offset and noise, and lower kickback noise. It is suitable for high- speed high-resolution SAR ADCs. As an example, the proposed modified version is suitable for the time-interleaved noise- shaping SAR ADC. As pointed out in, its ADC speed is limited by the comparator speed, and its ADC resolution is limited by

the comparator kickback noise. Although use a channel isolation to reduce the influence of kickback noise, this isolation increases the complexity of system. By contrast, the proposed modified version of three-stage comparator can solve these issues. It has the fastest speed and the smallest kickback noise compared to other comparators.

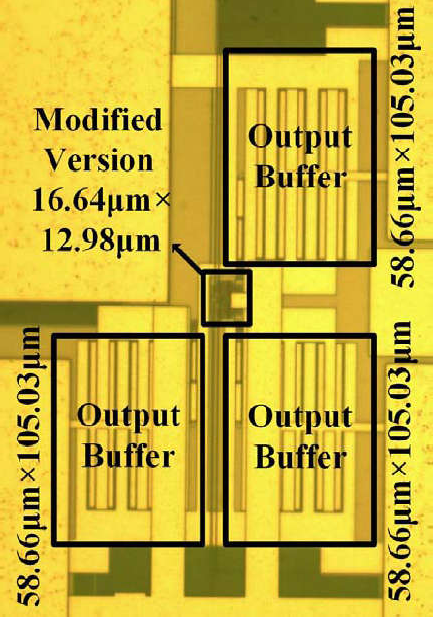
# RESULT ANALYSIS

In this paper, presents A Three-Stage Comparator And ITS Modified Version With Fast Speed And Low KICKBACK. This phase uses the tool used for simulation purpose for the research work is tanner tool version 8.3. This section compares the three-stage comparators of this work with the two-stage comparators of Miyahara’s comparator and Elzakker’s comparator. Despite the larger power consumption, the three-stage comparators have key advantages over the two-stage comparators. For example, the two-stage comparators cannot have a faster speed than the three-stage comparators, even if their power consumption is increased. This is due to the limitation in speed and power tradeoff. The larger power consumption means larger transistor sizes, and leads to larger parasitic capacitances. This means that the speed can hardly be further increased, even with a larger power consumption. By contrast, the three-stage comparators effectively increase the speed through larger power consumption. This is the advantage of the three-stage comparators. Overall, the key highlight of the three-stage comparators is the increased speed and the reduced kickback. And this is not at the cost of increased input referred offset or noise.

All the four comparators are fabricated in the same 130-nm process. Fig. 4 shows the die photographs of the three-stage comparators.



**Fig.4: Three Stage Comparator**



**Fig. 5: modified version of three-stage comparator.**

Table 1 compares this work with the state- of-the-art works. As can be seen, the three- stage comparator and its modified version have the smallest delay. The modified

version has the smallest kickback noise as well. The power consumption and area are also smaller than, regardless of the increased circuit complexity.

**TABLE.1 COMPARISONWITH STATE-OF-THE-ARTWORKS**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | [2]\* | [5] | [6] |  | Miyahara\* | | Elzakker’s\* | Three-Stage | Modified Version |  |
| Technology | 64 | 180 | 180 | 130 | | | | | | |
| Supply  Voltage(Vm) | 1.2 | 1.2 | 1.8 | 1.2 | | | | | | |
| Area(um2) | 125 | 392 | 490 | 89 | | 119 | | 161 | 316 | |
| Low-Kickback  Noise | NO | NO | NO | NO | | NO | | NO | NO | |
| Input  Offset(mV) | - | 8.8 | 2 | 18 | | 19 | | 14 | 12 | |
| Energy  Comparison(pJ) | 0.035 | 0.677 | 0.45 | 0.110 | | 0.112 | | 0.139 | 0.215 | |
| Input Noise(mV) | 0.5 | - | - | 0.55 | | 0.56 | | 0.58 | 0.54 | |
| Delay | 1245ps @ Vcm  =0.6v,  *V*id =1 mV | 560  ps @  Vcm  =0.6v,  *V*id =1 mV | 301  ps@  Vcm  =0.6v,  *V*id =1 mV | 307 ps@ Vcm =0.6v, *V*id =1 mV | | 312 ps@ Vcm =0.6v, *V*id =1 mV | | 234 ps@ Vcm =0.6v, *V*id =1 mV | 210 ps@ Vcm =0.6v, *V*id =1 mV | |

# CONCLUSION

his paper introduces a three-stage comparator and an enhanced version designed to achieve high speed, minimal kickback noise, and reduced input-referred offset and noise. These designs are particularly well-suited for high-speed, high-resolution SAR ADC applications. The effectiveness of the proposed comparators is supported by measured results.

In the proposed design, a PMOS latch, a PMOS preamplifier, and a small cross-coupled circuit are utilized. A specialized clocking scheme is employed to regulate the gain of the preamplifier. This clocking approach ensures adequate preamplifier gain. The use of PMOS transistors at the latch input, along with the cross-coupled circuit, maintains the preamplifier output's common-mode voltage at a low level.

The three-stage comparator and its modified version exhibit notable benefits, including high speed, low kickback noise, and reduced input-referred noise and offset. These features make them ideal for high-performance SAR ADCs. Measured results confirm the effectiveness and reliability of the proposed designs.

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