Cascaded H-Bridge Multilevel Inverter with Reduced Switching Topology

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| NIVETHA C K  UG Scholar, Dept of EEE St. Joseph’s College of EngineeringChennai, India [cknivetha09@gmail.com](https://d.docs.live.net/aec1ffae62dc27b4/Desktop/cknivetha09@gmail.com) | POOJA T M  UG Scholar, Dept of EEE St. Joseph’s College of EngineeringChennai, India [tmpooja.prema@gmail.com](https://d.docs.live.net/aec1ffae62dc27b4/Desktop/tmpooja.prema@gmail.com) | Dr.S.SRIDHARAN M.E.,Ph.D., Associate Professor, Dept of EEE St. Joseph’s College of EngineeringChennai, India [sridharans@stjosephs.ac.in](https://d.docs.live.net/aec1ffae62dc27b4/Desktop/sridharans@stjosephs.ac.in) |

***Abstract*— This paper presents Cascaded H-Bridge Multilevel Inverter with reduced switching topology. Cascaded H-bridge (CHB) Multi Level Inverter (MLI) holds the benefits in the availability of isolated DC links. This topology of CHBMLI is being frequent at usage in the renewable applications. To avoid the switching loss, the main purpose of MLIs lies in the usage of switches. Henceforth, to cope up with the problem, the number of switches is compulsorily increased for the higher level. This project presents the performance of Cascaded Diode Bridge Integrated H-Bridge Multilevel Inverter having thirteen levels. This technique is based on obtaining the pulses by comparing the sine wave with constant dc source of variable amplitude. With this technique, can reduce the frequency of PWM signal and therefore reduce the switching loss of power switches and harmonic components. MATLAB simulation results of this technique shows that THD are reduced to minimum value.**

***Keywords— Cascaded H-Bridge Multilevel Inverter, of Cascaded Diode Bridge Integrated H-Bridge Multilevel Inverter***

# Introduction

Over the last few decades, multilevel inverter (MLI) topologies have gained popularity in industrial application because of the superior power quality compared to its conventional two-level counterpart. For low and medium voltage/power applications, MLI find their applications in almost every field of electrical engineering including renewable energy systems, HVDC applications, distributed generation (DG)system, industrial drive applications, uninterruptible power supplies, etc. They are widely used in drives and other allied areas in industries. MLI’s are an assembly of power semiconductor devices along with different dc links to achieve staircase waveform close to sinusoidal at the output. For the sake of multilevel inverter, three distinct topologies have been proposed, which are: Diode-clamped (neutral clamped), Capacitor-clamped (flying capacitor), Cascaded H Bridge and modified cascaded H-Bridge. The CHBMLI uses capacitors and switches and uses less number of components at each level. This topology comprises of series of cells meant for power conversion and by that way, power can be easily scaled. The design of MLI mainly depends upon the number of levels required at the output, number of semiconductor devices used, number of dc voltage sources and capacitors utilized, modularity of topology and the total standing voltage (TSV) of topology. Beside all these, many other modulation and control strategies have been proposed or adopted for MLIs including these: Multilevel sinusoidal pulse width modulation(PWM), Multilevel selective harmonic elimination and space vector modulation (SVM). This proposes model after thorough investigation and modeling of different contemporaries Multilevel Inverters. Proposed model uses 8 MOSFETs, 3 DC sources to produce a stepped output waveform having 13 levels. The proposed model is able to achieve a low THD in the open loop system. Proposed Model provides superior waveform quality by maintaining pristine ideal sine wave quality for PV array to be interconnected to grid. Lastly, future work on proposed model is discussed in brief.

# CELL DESCRIPTION

Cell diagram is shown in Figure1. Each single cell holds one DC source and H-Bridge consists of four switches affiliated two switch in each arms and these two arms are connected parallel to each other.

Figure1 shows four switches S1, S2, S1’, S2’ forming the

H -Bridge.

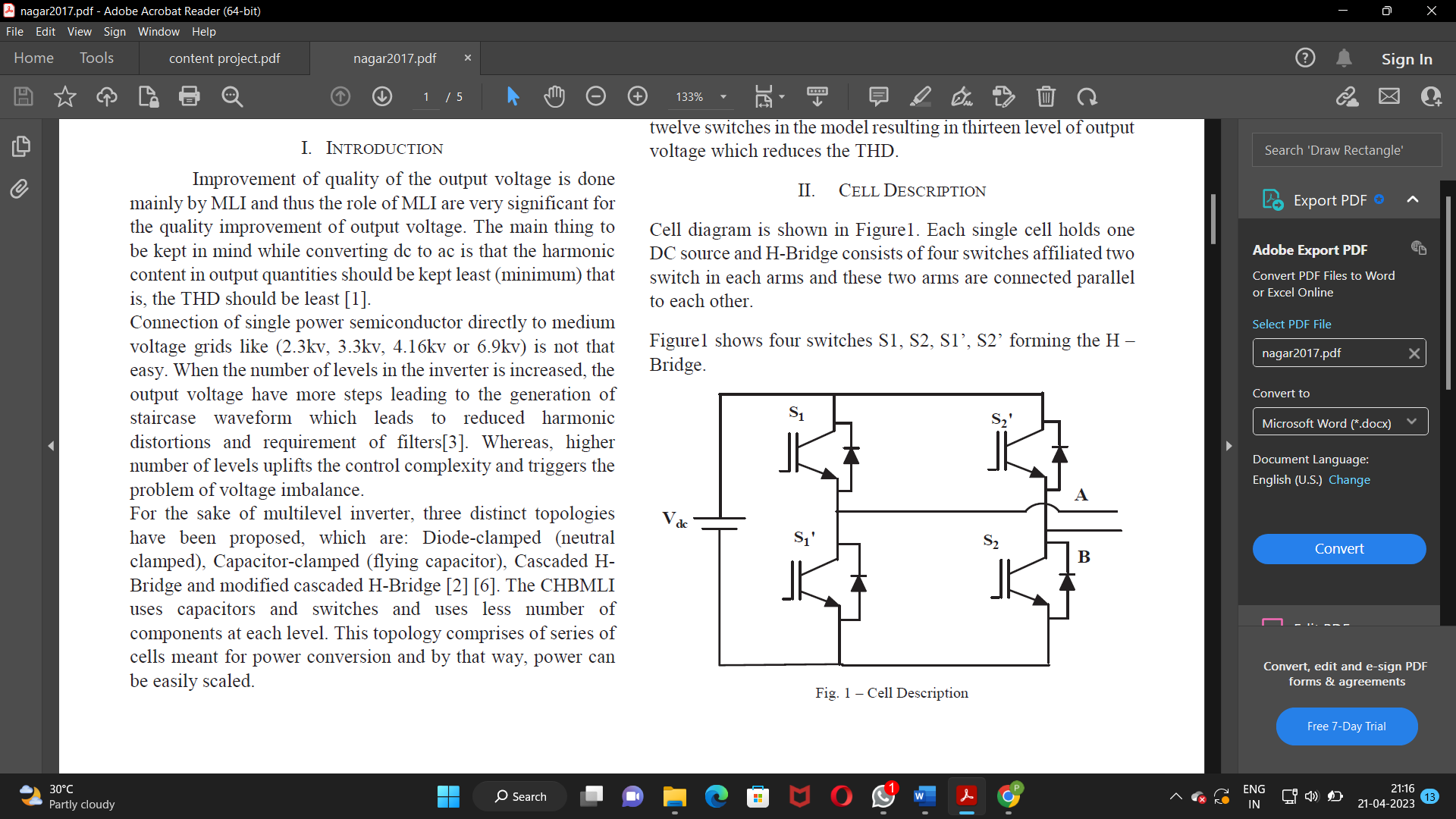


Fig 1. Cell Description.

This cell is also called single phase voltage source inverter and it is able to receive three level in output voltage. Now for the single phase five level VSI two single phase full bridge inverters with separate DC source are required [2][7].

All Voltage source inverters are capable of producing voltage levels 0, +Vdc, -Vdc. In proportional form for ‘x’ counts of bifurcated DC source, the output voltage level will be 2x+1.

Thus two bifurcated DC source produce voltage level of +2Vdc,-2Vdc, +Vdc, -Vdc and 0 in symmetrical mode [1].

Therefore if two cells are connected in cascaded manner it gives five level in the output voltage and total eight switches are present in model. Similarly for 13 level output voltage we can achieve by using this cells.

# PROPOSED SYSTEM

The proposed system is aimed to provide a detailed analysis of 13 level inverter with higher efficiency. The principle of operation of the 13-level inverter is to synthesize the output voltage of each module to form a step-like ac voltage waveform across the output terminal. The ac voltage is produced by adding the output voltage of each module with different duty cycles. In general, with higher number of H-bridge modules in a single-phase structure, there will be more levels in the ac output voltage; thus producing an ac waveform closer to a sinusoidal wave.

The hardware includes Multilevel Inverter with 8 MOSFETs, 3 DC sources to produce a stepped output waveform having13 levels.

Proposed model uses 8 MOSFETs and 3 DC sources to produce a stepped output waveform having 13 levels. The Proposed Cascaded H-bridge model with separate DC source is which uses much lesser switches as compared with conventional cascaded H- bridge and simpler control methods. Since the number of DC sources can be chosen arbitrarily, it is convenient to increase the step level of the output voltage and output power by cascaded H-bridge.

The circuit is proposed for 13- level voltage source inverter consisting of an H-bridge formed by 8 MOSFETs. There are 3 different DC sources connected to circuit and 8 MOSFETs to control the step voltage level across the load terminals**.**

The principle of operation of the 13-level inverter is to synthesize the output voltage of each module to form a step-like ac voltage waveform across the output terminal. The ac voltage is produced by adding the output voltage of each module with different duty cycles. In general, with higher number of H-bridge modules in a single-phase structure, there will be more levels in the ac output voltage, thus producing an ac waveform closer to a sinusoidal wave. The number (M)of ac output voltage levels is given by M = 2N+1, where N is the number of PV cells/modules.

In an H-bridge there are two modes of operations depending on the pattern of the switching signals. The fundamental operation principle of the cascaded H-bridge multilevel inverter relies on the second mode of operation. In this mode, four switches in the H-bridge module is switched in four different sequences to generate a 3-level output voltage across output terminal of each H-bridge module.

In comparison with the conventional CHB multilevel inverter, the proposed topology uses lower number of components.

For the 13-level inverter, the proposed topology uses only 11 switches while the CHB multilevel inverter uses 16 switches for the same number of voltage levels. The proposed topology shows some advantages in comparison with the 5-level coupled-inductor inverter presented in the topology presented in uses 8 switches for generating 5-level voltage while the proposed topology uses 11 switches (only two more switches) for generating 13-level voltage. Also, in the topology of the maximum output voltage is limited to half of the value of the dc voltage source.

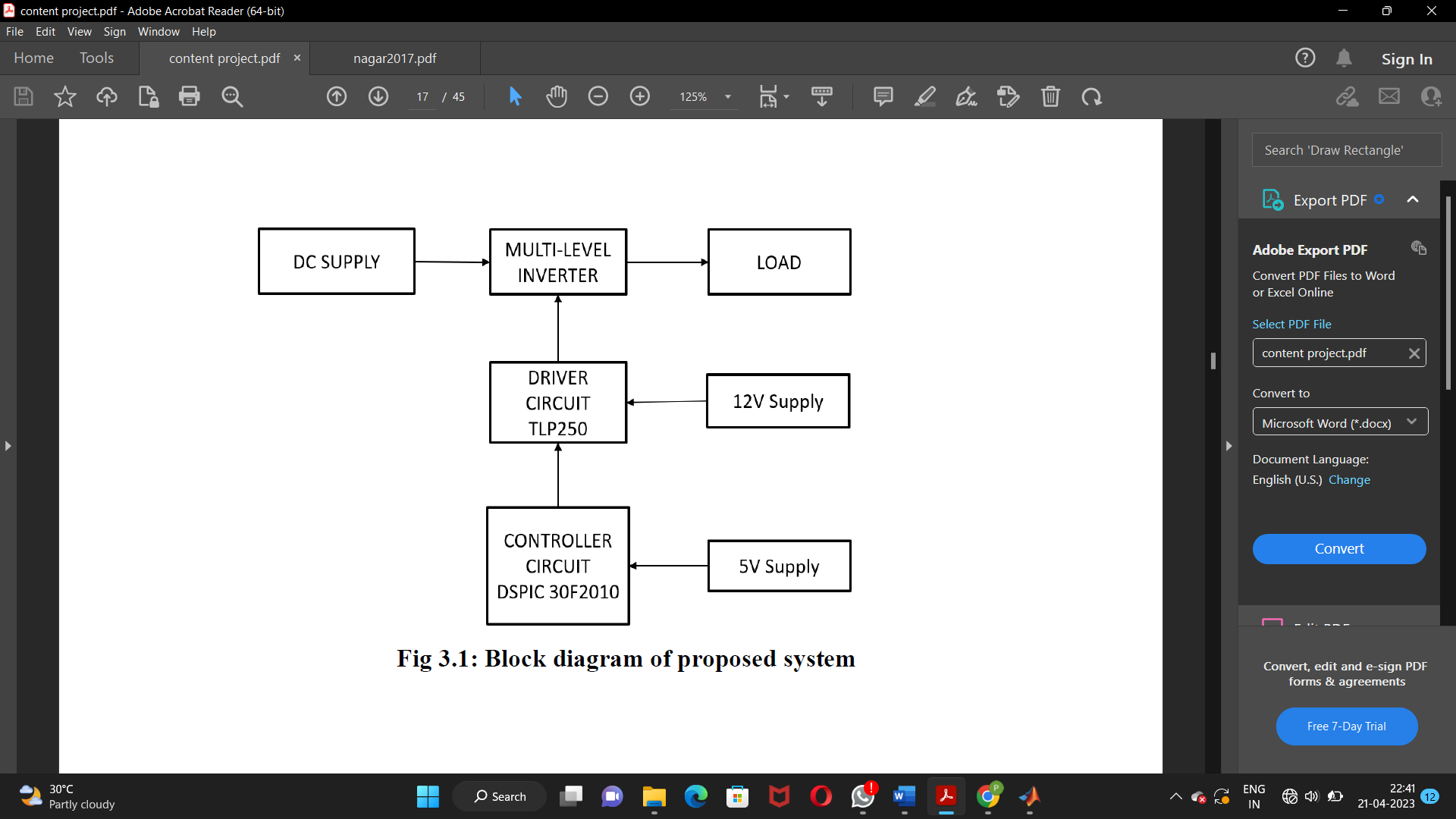


Fig 2.Block Diagram

# SIMULATION

The simulation mimics the operation of cascaded h bridge multilevel inverter providing evidence for decision making by being able to test different scenarios and processed changes this can be also coupled with virtual reality technologies for more immersive experience. It provides us with critical analysis of indulged information.

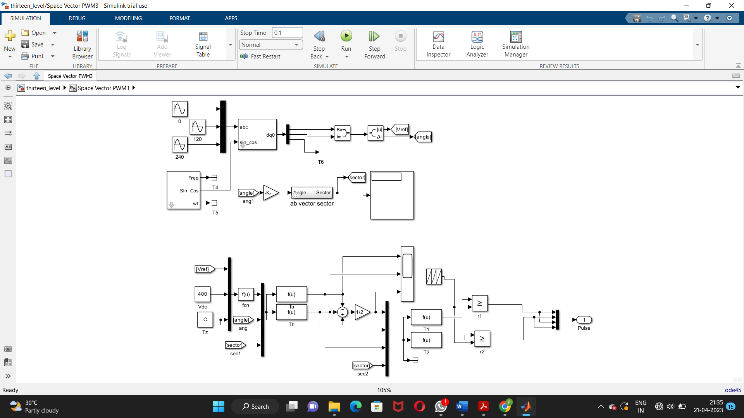
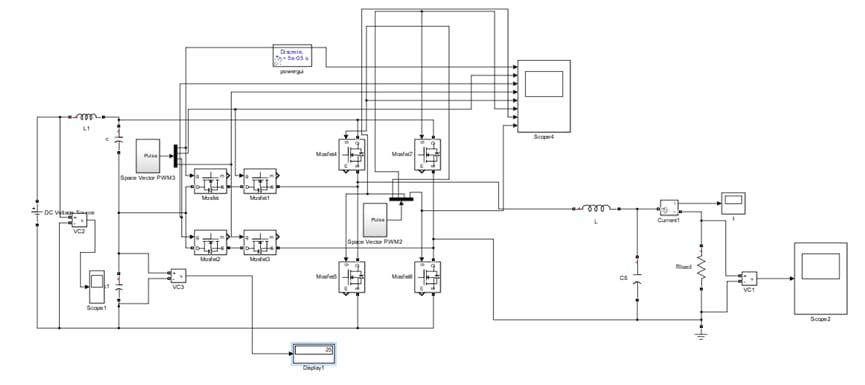
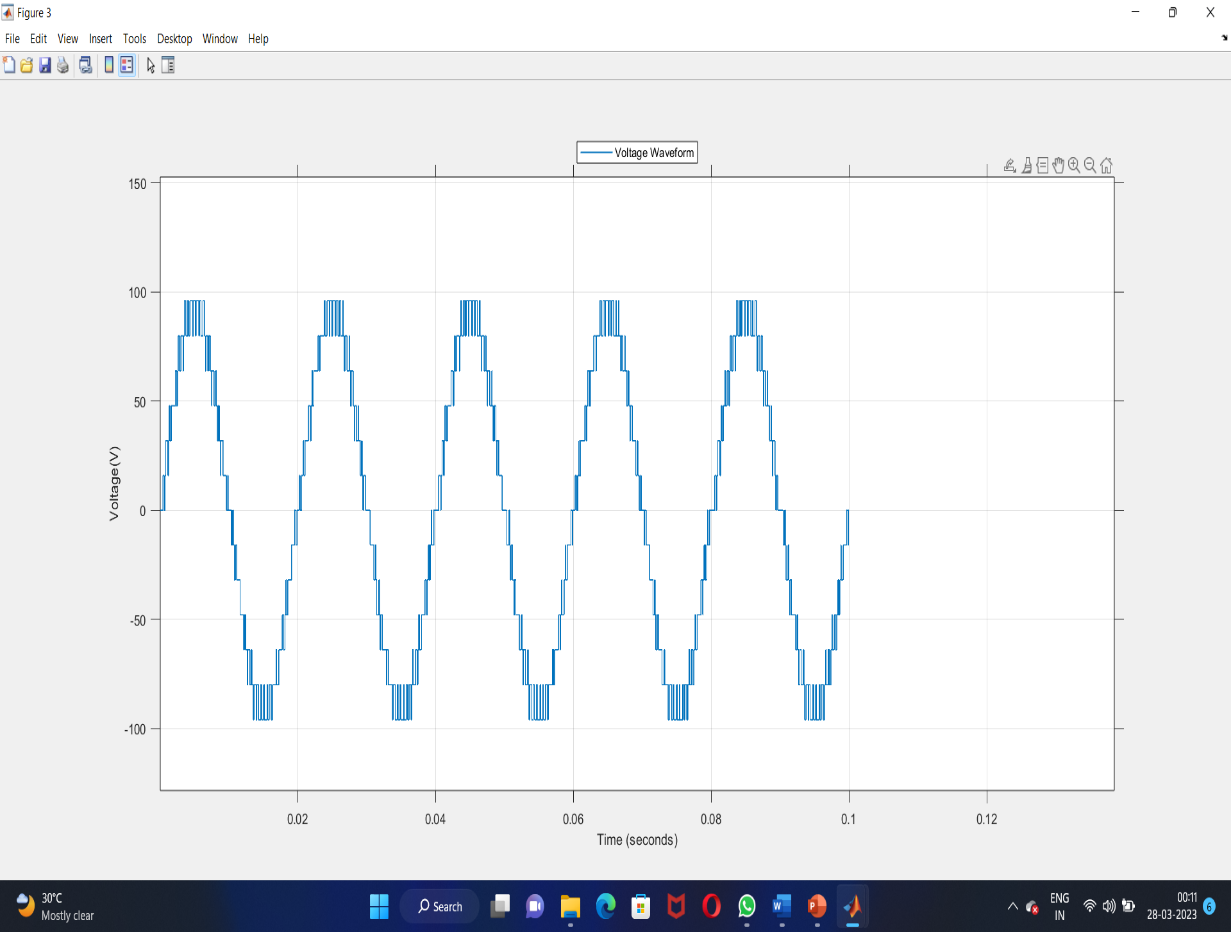


Fig 3. Sub System

## Simulink Model



## Output Voltage Waveform



# MODULATION TECHNIQUES

Key modulation techniques for multi-level inverter are:-

• Multi-Level Sinusoidal / Multi-Carrier PWM

• Space Vector (SVM) PWM

• Selective Harmonic Elimination (SHE)

Multi-Carrier Sinusoidal PWM technique is known because of its good quality output generation capability and simplicity. This technique is classified into –

• Level Shifted PWM

• Phase Shifted PWM

• Hybrid PWM

These techniques are further classified as shown below:-

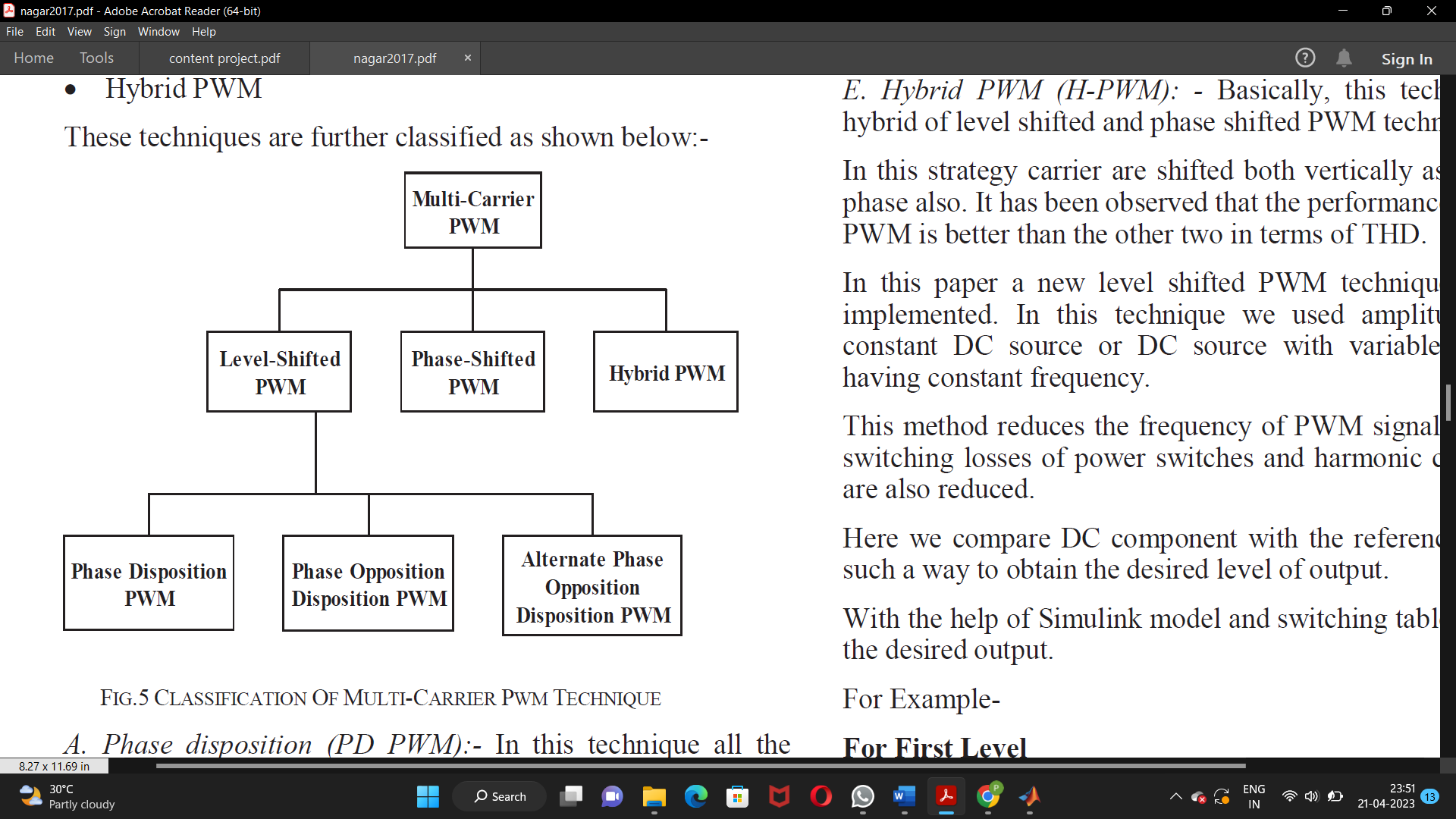


Fig 6. Classification of PWM Techniques

## Phase disposition (PD PWM):-

In this technique all the modulating signals are in phase, and a sinusoidal reference signal is continuously compared to producing the gating signals.

## Phase opposition disposition (POD PWM):-

In this category of level shift PWM technique modulating signal above the reference (zero) line is 180 degrees out of phase with modulating carrier signals below the reference line.

## Alternate phase opposition disposition (APOD PWM):-

In this PWM strategy, every modulating carrier waveform is out of phase with its neighbour modulating carrier by 180 degrees.

## Phase-shifted (PS PWM):-

This technique is mainlyemployed to produce the multi-level stepped waveform of output voltage with lesser total harmonic distortion (THD). In this modulation strategy, all of the triangular carriers have the same value of peak to peak amplitude and also have same frequency The gate signals for MLI switches are produced by comparing the carrier triangular waveform with reference sinusoidal waveform.

Multi level inverter with N number of levels involves (N-1)

number of triangular carriers.

*E. Hybrid PWM (H-PWM): -*

Basically, this technique is a hybrid of level shifted and phase shifted PWM technique. In this strategy carrier are shifted both vertically as well as in phase also. It has been observed that the performance of Hybrid PWM is better than the other two in terms of THD.

In this paper a new level shifted PWM technique has been

implemented. In this technique we used amplitude shifted

constant DC source or DC source with variable amplitude

having constant frequency. This method reduces the frequency of PWM signals therefore, switching losses of power switches and harmonic components are also reduced. Here we compare DC component with the reference signal in such a way to obtain the desired level of output. With the help of Simulink model and switching table we obtain the desired output.

For Example-

**For First Level**

Switches sa3, sa4, sb4 and sb6 conducts and we obtain 100 V in the output.

**For Second Level**

Switches sa4, sa6, sb4 and sb6 conducts and we obtain 200 V in the output.

**For Third Level**

Switches sa4, sa6, sb4 and sb5 conducts and we obtain 300 V in the output.

**For Fourth Level**

Switches sa4, sa5, sb4 and sb5 conducts and we obtain 400 V in the output.

**For Fifth Level**

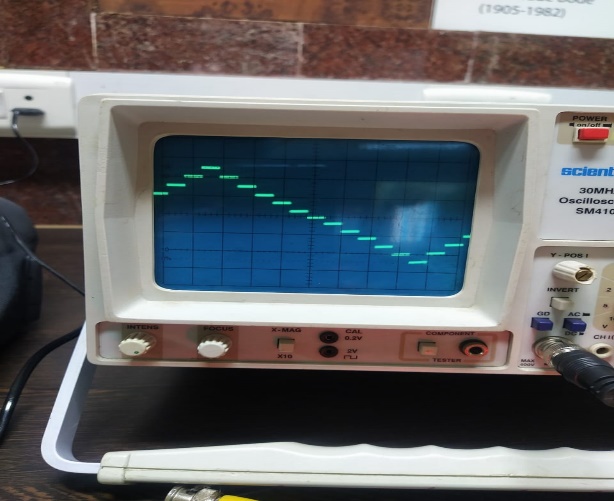
Switches sa4, sa5, sb1 and sb4 conducts and we obtain 500 V in the output.Similarly the process goes on and we obtain the thirteen level output.

# HARDWARE IMPLEMENTATION AND RESULTS

The principle of operation of the 13-level inverter is to synthesize the output voltage of each module to form a step-like ac voltage waveform across the output terminal. The ac voltage is produced by adding the output voltage of each module with different duty cycles. In general, with higher number of H-bridge modules in a single-phase structure, there will be more levels in the ac output voltage, thus producing an ac waveform closer to a sinusoidal wave.

The hardware makes use of highly efficient CHB architecture over other due to its reduced harmonic content and eradication of filter circuit. The highly efficient control technique space vector pulse width modulation is implemented. Due to its fixed switching frequency, low harmonic content and higher DC bus utilization.





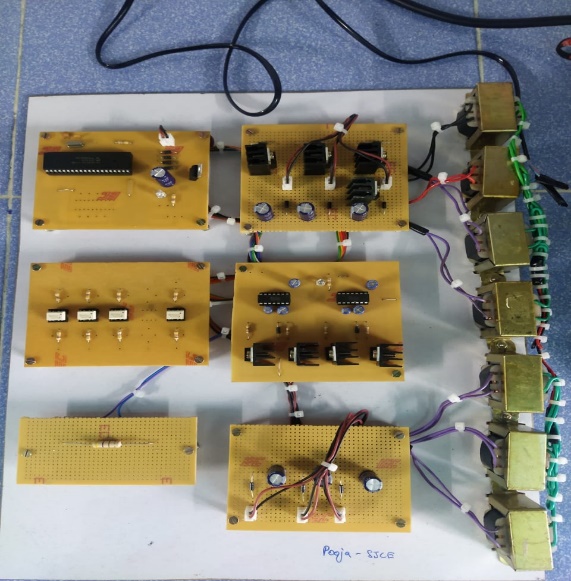


Fig 7. Hardware implementation of proposed system

VII . CONCLUSION

Thus the implementation of Cascaded H-Bridge Multi level Inverter with MOSFET switches that produces 13 level output with high power quality, increased voltage efficiency, reduction in THD, increased density is developed and its simulation results are exhibited. It improves the output level of inverter, provides flexibility in design and also decreases the harmonic content. The performance of inverter has been verified with the help of simulation using MATLAB. The Line voltage and line current THDs with this techniques in both cases are determined and it is observed that there is no significant difference.

FUTURE SCOPE

The THD can be further reduced by increasing the inverter levels. More efficient control technique space vector modulation is implemented as it possess fixed switching frequency low harmonic content and higher DC bus utilization. This can be used for further implementation of various hardware circuits. Modification in filter design for implementation of highly efficient output voltages.

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