**Using LT Spice tools, design and perform a first-order sigma-delta modulator simulation.**

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**ABSTRACT**

A single-phase Sigma-Delta ADC with a first-order rectifier and switched capacitors is proposed. The first low-power production ADC application provides a 1-bit Sigma-Delta data transfer capability to recognize a 10 MHz input signal. The ADC is a function of this circuit. Design, simulation, and analysis of a 1-bit (L-1") first-order Sigma-Delta modulator using a 1.8 V, 250 nm CMOS power supply from LTspice The robustness, high performance, and stability show better performance, the current and sigma-delta areas are smaller, and the simulation is compared with the conventional ADC simulation.

**Keywords:** ADC, DAC, LT spice, CMOS, sigma .

1. **INTRODUCTION**

Transistor sizing advances technology in semiconductors. Moore's Law: doubling transistors = more capabilities in ICs = growth in the semiconductor industry. More transistors = more integrated functions over time. The growth is driven by transistor miniaturization and manufacturing advancements. An AID device changes analog voltage signals to digital ones, while analog signals dominate real-world communications [1]. But digital signals are essential for some applications, such as digital signal processing. Mechanical improvements in computerized VLSI circuits have expanded the requirements for minimum costs, high-performance auxiliary transformers, and DIA (Advanced to Simple), many of which are simple devices coordinated with computerized ones [2]. Noise coupling issues hinder the integration of sensitive analog and digital circuits on one chip. Sigma-delta modulation (SDM) overcomes delta modulation limitations. It summarizes differences between previous and current signals [3] .

1. **SIGMA-DELTA ARCHITECTURE'S OPTIMAL TOPOLOGY**

Oversampling converters do not require a sample-and-hold circuit because they typically use switched-capacitor circuits. In Figure 1, the sigma-delta modulator is shown. It is under the category of sample converters. To determine whether this new sample is greater than the previous sample, the comparator compares the input signal with the previous sample. The larger the output, the smaller it is, and vice versa. This process is called "delta adjustment" because the Greek letter "1" (delta) is used to represent small deviations or gradations. The process of measuring signal change between samples is what creates delta waves, which are then used to modulate an analog signal. advanced sigma-delta modulator design; It mainly consists of an integration unit. The order of modifiers in a direct path is determined by the number of modifiers present in that path. A 1-bit DAC sends the comparator output back to the collector input, creating a negative feedback loop that drives voltage to VIN. The DAC's average output voltage equals Vin [5]. The 1-bit DAC, a multiplexer circuit controlled by the comparator, determines the input's sum of +Vref or –Vref [3]. When the output of the integrator is greater than the reference voltage at the input of the comparator, the comparator provides an "output high" signal. The high output controls the DAC, leading to a +Vref output that offsets the modulator input for an opposite integration output shift. The critical path shifts the integrator output positively if it differs from the comparator input's reference voltage. The integrator approximates the output to zero by summing the difference between the input and quantized output signals [4].

Comparator

1-BITSerial Data

**Figure 1:** 1-bit sigma-delta modulator.

1. **THE IMPLEMENTATION OF OPERATING AMPLIFIER**

At the heart of the sigma-delta modulator is an operational amplifier. This provides a great open-loop advantage for implementing negative review ideas and allows integrators to coordinate seamlessly. Wide bandwidth for handling the initial two sine wave harmonics. As the differences build up over time, the op amp operates at clock speed. The subwoofer's gain-bandwidth product should exceed 1 for efficient signal transmission at clock speed. Figure 2 depicts the op amp's utilization. The first stage has two differential pairs, one current mirror for each pair, and two current mirror loads. It converts the differential supply into a single-ended supply with high differential gain. In addition to shifting the differential to one end, this step provides a large differential gain. The n-channel combined source amplifier MS and the p-channel load current M6 form the second stage. Transistors MS and M9 provide bias to the op-amp circuit. The operational amplifier voltage varies from +2V to -2V and has a gain bandwidth (GB) of 10MHz. The ref current is sourced by transistors M5 and M9 [8], resembling a resistive diode set [5]. It has a power dissipation of 18.23 W and an output impedance of 1K. Ref's frequency response can be seen in Figure 3.



**Figure 2:** Diagram of an operational amplifier.

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**Figure 3:** The Op-frequency Amp's response (Input & Output).

1. **THE COMPARATOR'S DESIGN**

The first-order scale is comparative. Since the comparison is 1-bit, it has only two levels: "1" or "0". Vdd = + 1 is implied by "1". Vss = -1. SV is represented by SV and "0". If the output of the combiner is greater than the reference voltage (Vref), then the output will be "1" [7]. If the output of the combiner is less than the reference voltage (Vref), then the output will be "0" [6]. The required function is performed efficiently using a simple comparator. The operational amplifier can perform the comparator function. The comparator only switches between supply rails; no compensating network is needed. Since pinning only delays the change, it is not necessary. Sine wave in circuit switches comparator rails To determine the speed of the comparator, provide a step input and observe its response time. The base clock frequency relies on the maximum comparison number speed. Clock frequency doesn't always lead to many comparisons. The clock rotates from -2.5V to +2.5V in half a revolution. Distortion occurs if the clock frequency exceeds 10 MHz, the maximum allowed as per the flowchart above. The comparator's transient response, with a 0.5V offset, is displayed in Figure 5.



**Figure 4:** Diagram of the Comparator.



**Figure 5:** Comparator's frequency response (Input & Output).

1. **THE 1-BIT DAC'S DESIGN**

The DAC gets a 1-bit input from a CMOS op-amp. A computer-controlled converter then changes the result into a symbol and feeds it back to the integrator. The DAC has 2 transmit ports. Vref signals are chosen based on input. The voltage reference is crucial for converting digital to analog. This figure 6 shows a 1-bit digital-to-analog converter (DAC), with two reference voltage levels (+2.5 volts and -2.5 volts). A DAC adjusts the output voltage so that the feedback loop matches the input voltage. The difference between the two is then divided equally, producing the frequency response shown in Figure 7. A 1-bit DAC can use a multiplexer to choose between +Vref and -Vref signals as the input signal is a 1-bit digital value.



**Figure 6:** Diagram of the DAC



**Figure 7:** The input and output of DAC's frequency response

1. **RESULT AND SEMILUSTION**

The first-order modulation quantizer is a comparator. The comparator only has 1 bit (1" or "0"), so there are only 2 stages. When used with MOS SPICE level 1 model parameters, LTspice simulation (LTspice IV.4.21b linear technique, SPICE simulator) provides theoretical results. 250nm CMOS technology was used to create the main operational amplifier circuit, comparator, and sigma-delta DAC (IL'-.ADC). Figure 8 displays sigma-delta ADC frequency response. It's well-known in conventional first-order ADC with input frequencies up to 10 MHz and Vdd = +1.8 V and Vss = -1.8 V. Rauschen 6.15NI uses 35,426 watts power.



**Figure 8:** The 1-BitSigma­ Delta ADC's frequency response

1. **CONCOLUTION**

Based on the standard 250nm n-well CMOS process, a first class Sigma-Delta ADC is built. Using the Sigma-Delta modulator, it has been shown that even a weak analog signal can be converted to a high-fidelity digital output. Switched-capacitor circuits are useful for designing low-voltage, high-precision sigma-delta rectifiers when high-voltage transistors are the only option. It has been observed that reducing the oversampling ratio has little effect on reducing the power loss of the modulator.

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