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CASCADED SWITCHED-CAPACITOR MULTILEVEL INVERTER

Komatipalli Siva Prasad[1], A Ravi[2]

[1]PG student, Thandrapaparaya institute of science and technology, Bobbili, AP india

[2]Asst.Professor, Department Electrical and Electronics Engineering, Thandrapaparaya institute of science and technology, Bobbili, AP india

ABSTRACT

Proposed topology consists of a new switched-capacitor dc/dc converter (SCC) which has boost ability and can charge capacitors as self-balancing by using proposed binary asymmetrical algorithm and series-parallel conversion of power supply. Proposed SCC unit is used in new configuration as a sub-multilevel inverter (SMLI) and then, these proposed SMLIs are cascaded together and create a new cascaded multilevel inverter topology which is able to increase the number of output voltage levels remarkably without using any full H-bridge cell and also can pass the reverse current for inductive loads. Switched-capacitor multilevel inverters (SCMLIs) which can generate a great number of voltage levels with optimum number of components for both symmetric and asymmetric value of dc voltage sources. In this case, two half bridges modules besides two additional switches are employed in each of SMLI units instead of using a full H-bridge cell which contribute to reduce the number of involved components in the current path, value of blocked voltage, the variety of isolated dc voltage sources and as a result the overall cost by less number of switches in comparison with other presented topologies. The validity of the proposed SCMLI has been carried out by several simulation and experimental results.

Keywords: Cascade sub-multilevel inverter, series parallel conversion, self-charge balancing, switched capacitor.

1. INTRODUCTION

Electricity plays an important role in modern society since it was first used about one century ago. To utilize electricity for all kinds of tasks, many different electrical and electronic devices have been invented. Among these, the DC-AC converter is one of the most important power electronic devices. One of the most widely used strategies for controlling the AC output of power electronic converters is the technique known as pulse width modulation (PWM), which varies the duty cycle of the converter switches at a high switching frequency to achieve a target average low-frequency output voltage or current. A traditional sine-triangle PWM is shown in Figure1.1.

Three significantly different PWM methods for determining the converter switching ON times have been usefully proposed for fixed-frequency modulation systems. These PWM methods are:

1. Naturally sampled PWM: Switching at the intersection of a target reference waveform and a high-frequency carrier.
2. Regular sampled PWM: Switching at the intersection between a regularly sampled reference waveform and a high-frequency carrier.

Direct PWM: Switching so that the integrated area of the target reference waveform over the carrier interval is the same as the integrated area of the converter switch

Other PWM methods are variations of these three basic PWM methods. Even the well-known space vector modulation strategy, which is often claimed to be a completely different modulation approach, is really just a variation of regular sampled PWM which specifies the same switched pulse widths but places them a little differently in each carrier interval.

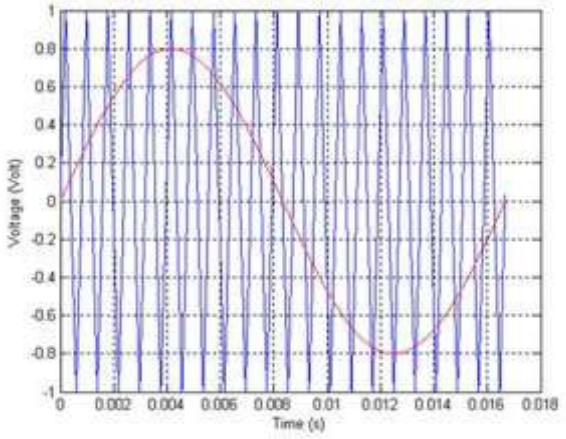

Figure 1.1: Sine-triangle PWM control (a) sinusoidal reference signal and triangle carrier signal;

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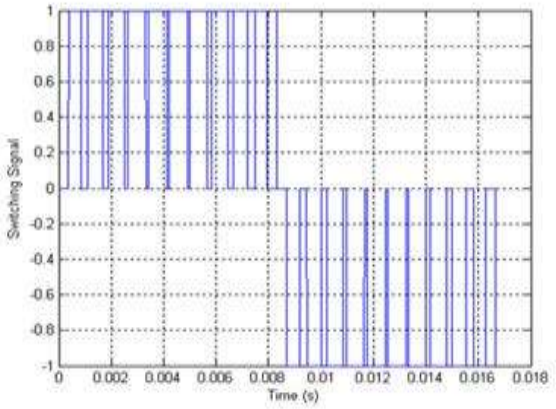

(b) switching signal

2. MULTILEVEL INVERTER

Numerous industrial applications have begun to use high power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power levels. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel inverter structure has been introduced as an alternative in medium and high power applications. With this type of inverters, improvements in the harmonic quality of the output voltage can be achieved. Multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources.

Renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel inverter system for medium and high power applications. Multilevel inverter produces a desired AC voltage waveform from several levels of DC voltages. These DC voltages may be or may not be equal. AC voltage produced from these DC voltages is of stepped waveform. One drawback of using multilevel inverter is to approximate sinusoidal waveforms from stepped waveform. The staircase waveform produced by the multilevel inverter contains sharp transitions. Fourier series theory makes clear that this phenomenon results in harmonics, in addition to the fundamental frequency of the sinusoidal waveform. The power quality of the power system is affected by the harmonics generated on the AC side. The power quality of the multilevel inverter is improved by performing the power conversion in small voltage steps. Multilevel inverter widely replaces the conventional two level three phase Voltage Source Inverter (VSI) by its performance such as lower switching stress (dv/dt) and lower THD on output voltage. The multilevel inverters start from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels is limited by voltage unbalance problems, voltage clamping requirement, circuit layout and packaging constraints. A multilevel inverter has several advantages over a conventional two level inverter that uses high switching frequency PWM. The attractive features of a multilevel converter can be briefly summarized as follows:

- Multilevel inverters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses. Therefore electromagnetic compatibility problems can be reduced.
- Multilevel inverters produce smaller CM voltage; Therefore, the stress in the bearings of a motor connected to a multilevel inverter drive can be reduced. Furthermore, CM voltage can be laminated by using advanced modulation techniques
- Multilevel inverters will draw input current with low distortion.
- Multilevel inverters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

The main drawback of multilevel inverters is that the number of switches increases with the number of levels. In early stages of multilevel inverters, development of control circuitry for large number of power switches was a significant problem. But continuous evolution of CPLD, DSP and FPGA devices easily solved this inconvenience. Other drawback of this inverter is the requirement of multiple numbers of DC voltage sources, mainly provided by capacitors. Balancing the voltage sources during operation under different load conditions is an important challenge. In spite of these drawbacks, introducing multilevel inverters will decrease switching losses occurred in the power device. By comparing with two level inverters, smaller size filter is required for the elimination of harmonics. This reduces the inverter weight, dimension and cost. Many multilevel inverter topologies have been proposed during the last two decades. Contemporary research has evolved novel inverter topologies and unique modulation schemes. MULTILEVEL inverters(MLIs) are known as one of the most popular solutions to improve the performance of renewable energy systems, electric vehicles (EVs) and other innovative power electronic utilities in medium and high power applications . These converters can

generate a staircase voltage waveform at the output with high quality and desired spectrum. The desired output voltage is synthesized by appropriate switching of several dc voltage links which leads to decrease voltage stresses on switches and total harmonic distortion (THD).

In general, there are three conventional types of MLI configurations categorized into diode clamped (DCMLI), flying capacitors (FCMLI) and cascade H-bridge topologies (CHB) which can be divided into two entire divisions based on symmetric and asymmetric value of dc power supplies. Although these converters have a lot of advantages over the classic inverters, using aforementioned conventional topologies needs more number of required power switches, power supplies and large capacitor banks. Furthermore voltage of the capacitors tends to be discharged theoretically and therefore charge balancing control processing is necessary. There have been several suggested charge balancing circuits to control the capacitors' voltage. could regulate the duty cycle of dc bus capacitors for FCMLIs by using the existing redundancy switching states (RSSs). In this case, the accuracy of proposed approach depends on designing a close loop control system. Also, presented a phase-shift modulation approach to obviate the discharging problem in a capacitor-based 7-level CHB topology supplied by one dc voltage source for main unit and one floating capacitor for auxiliary unit

Here, the main and auxiliary power switches have to drive by fundamental and high switching frequency, respectively. Meanwhile, presented a triplen harmonic compensatory method based on fundamental switching strategy to extend the range of modulation index for three phase utility of 7-level CHB topology. Using the resonant switched capacitor circuit (RSCC) as an external voltage balancing network can also prevent this problem for DCMLIs. Nowadays, many researchers have presented numerous developed structures of MLIs with less number of key components such as number of required switches, gate drivers, power supplies and so on . One of the most particular schemes of them is switched-capacitors multilevel inverters (SCMLIs). These converters can produce more output voltage levels with less number of required power supplies . SCMLIs contain several capacitors and switches which can connect dc power supply to ac output and are able to decrease the burden of power supply to achieve higher number voltage levels. Nevertheless, to attain the greater number of output voltage levels with less number of power semiconductors and simple commutation, a new type of SCMLIs have been emerged using the series/parallel switching strategy (SCISPC). The distinctive features of these types of inverters are that they can increase the flexibility of systems by switching between several capacitors in series or parallel modes and therefore can transfer more input power to the output. In this way, [27] and [28] presented a new family of cascade and hybrid SCISPC topologies which have a modular structure and generate more output voltage levels with least of switches. But such structures have used the full H-bridge units with isolated dc voltage sources to change the polarity of output voltage waveform which makes more conducting loss through the current path components and increases the number of power switches.

In this paper, initially a new switched-capacitor dc/dc converter (SCC) is presented which can switch as conventional series/parallel conversion and generate multiple dc link voltages with optimum components. In this case, voltage of all capacitors is filled by binary asymmetrical pattern without using any auxiliary circuits. At the next, a new sub-multilevel inverter topology presents which is performed based on proposed SCC unit and without using full H-bridge cell. In addition, this structure is suitable for an inductive load with capability to pass the reverse current. After that, proposed sub-multilevel modules are cascaded with each other and create more output voltage levels. Therefore most of the parameters such as number of required switches, diodes, maximum current path components and value of total blocked or standing voltage are improved. In order to prove the performance of the proposed circuit, variety number of comparisons with other recently suggested topologies has been done in fair conditions and also analysis of theoretical power losses is given.

Finally validity of the proposed topology is shown by several experimental and simulation results.

Diode-Clamped Converter:

The simplest diode-clamped converter is commonly known as the neutral point clamped converter (NPC) which was introduced by Nabaeet al. [4]. The NPC consists of two pairs of series switches (upper and lower) in parallel with two series capacitors where the anode of the upper diode is connected to the midpoint (neutral) of the capacitors and its cathode to the midpoint of the upper pair of switches; the cathode of the lower diode is connected to the midpoint of the capacitors and divides the main DC voltage into smaller voltages, which is shown in Figure 2.1. In this example, the main DC voltage is divided into two. If the point O is taken as the ground reference, the three possible phase voltage outputs are $-1/2V_{dc}$, 0, or $1/2V_{dc}$

The line-line voltages of two legs with the capacitors are: V_{dc} , $1/2V_{dc}$, 0, $-1/2V_{dc}$ or $-V_{dc}$. To generate a three-phase voltage, three phases are necessary.

The five-level output voltage can be generated by controlling the switches. Table 2-1 shows the proper switching states. The switches (S_{a1} and $S_{a'1}$) and ($S_{a2}$and $S_{a'2}$) are complementary pairs. When S_{a1} is on (S_{a1} = 1), $S_{a'1}$ is off ($S_{a'1}$ = 0).

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Other switch pairs are similar. Figure 2.2 shows a two-phase diode-clamped multilevel converter. Some disadvantages of the diode-clamped multilevel converter may be observed. Using extra diodes in series becomes impractical when the number of levels m increases, requiring (m-1)(m-2) diodes per phase if all the diodes have equal blocking voltages. Note that the voltages for diodes in different positions are not balanced. For example, diode D_{a2} must block two capacitor voltages, $D_{a(m-2)}$ must block (m-2) capacitor voltages. Also, the switch duty cycle is different for some of the switches requiring different current ratings. In addition, the capacitors do not share the same discharge or charge current resulting in a voltage imbalance of the series capacitors.

The capacitor voltage imbalance can be controlled by using a back-to-back topology, connecting resistors in parallel with capacitors, or using redundant voltage states [4].

The advantages for the diode-clamped converter are the following:

(1) A large number of levels yields a small harmonic distortion.

(2) All phases share the same DC bus.

(3) Reactive power flow can be controlled.

(4) Control is simple.

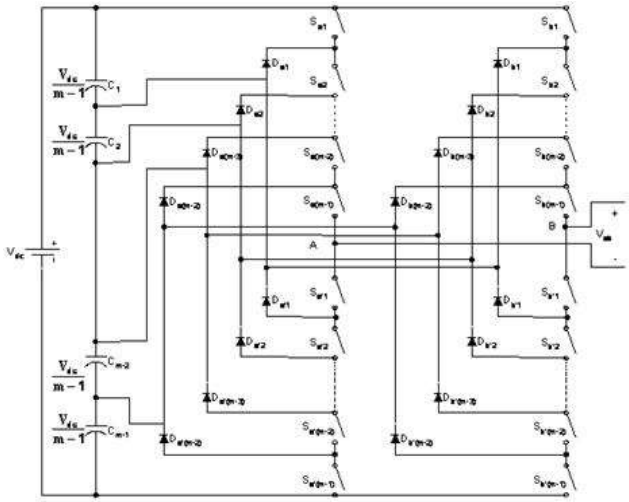

Figure 2.1: Neutral point diode-clamped converter

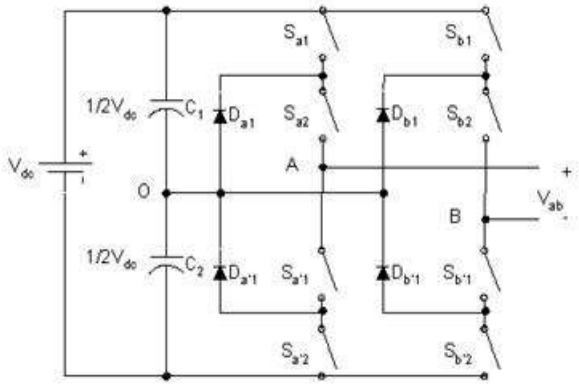

Figure 2.2: Two-phase diode-clamped multilevel converter

Table 2.1: Switch states and the output voltages for diode-clamped multilevel converter

S_{a1}	S_{a2}	$S_{a'1}$	$S_{a'2}$	S_{b1}	S_{b2}	$S_{b'1}$	$S_{b'2}$	V_{ao}	V_{bo}	V_{ab}
0	0	1	1	1	1	0	0	$-1/2V_{dc}$	$1/2V_{dc}$	$-V_{dc}$
0	0	1	1	0	1	1	0	$-1/2V_{dc}$	0	$-1/2V_{dc}$
1	1	0	0	1	1	0	0	$1/2V_{dc}$	$1/2V_{dc}$	0
0	0	1	1	0	0	1	1	$-1/2V_{dc}$	$-1/2V_{dc}$	0
0	1	1	0	0	0	1	1	0	$-1/2V_{dc}$	$1/2V_{dc}$
1	1	0	0	0	0	1	1	$1/2V_{dc}$	$-1/2V_{dc}$	V_{dc}

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The disadvantages are the following:

(1) Different voltage ratings for clamping diodes are required.

(2) Real power flow is difficult because of the capacitors' imbalance.

(3) Different current ratings for switches are required due to their conduction duty cycle.

Capacitor-Clamped Converter

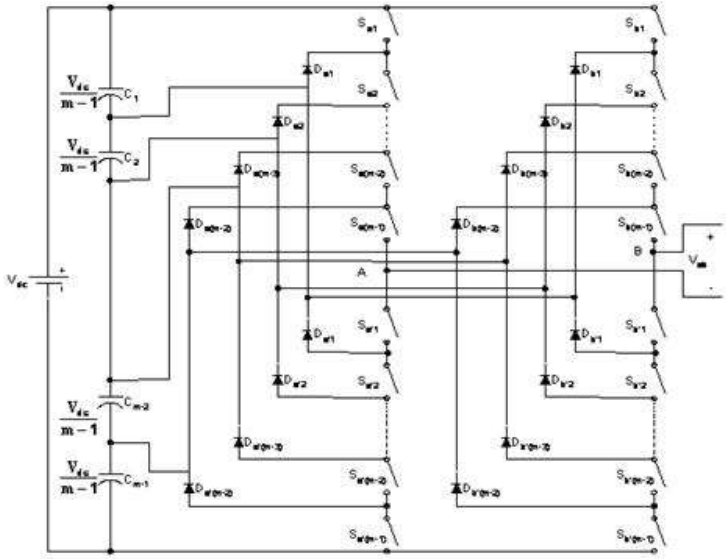


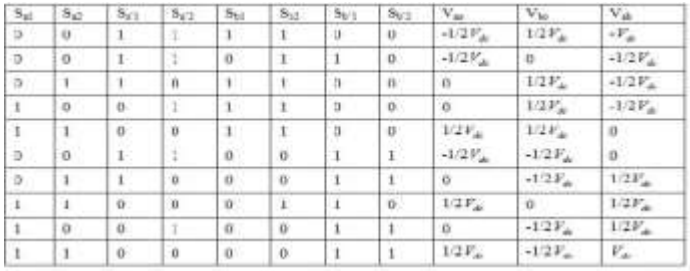
Figure 2.3: Topology of a capacitor-clamped multilevel converter

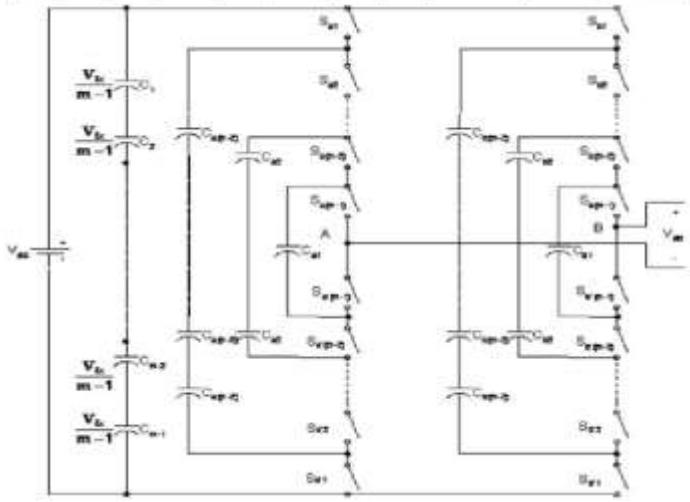
Table 2.2 shows the possible switch combinations to generate the five-level output waveform.

An output voltage can be produced by using different combinations of switches. The topology allows increased flexibility in how the majority of the voltage

levels may be chosen. In addition, the switches may be chosen to charge or discharge the clamped capacitors, which balance the capacitor voltage. The general m - level capacitor-clamped multilevel converter has an m-level output phase voltage. Thus, two phases would produce a (2m □1) level output voltage, or line voltage, which is shown in Figure 2.4. Similar to the diode-clamped multilevel converter, the capacitors have different ratings. These capacitors result in a bulky, and expensive converter when compared to the diode-clamped converter.

Table 2.2: Switch states and the output voltages for capacitor-clamped multilevel converter





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bridge is shown in Figure 2.5. A single H-bridge is a three-level converter. The four switches S_1, S_2, S_3 and S_4 are controlled to generate three discrete outputs

V_{out} with levels V_{dc} , 0 and $-V_{dc}$. When S_1 and S_4 are on, the output is V_{dc} ; when S_2 and S_3 are on, the output is $-V_{dc}$; when either pair S_1 and S_2 or S_3 and S_4 are on,

the output is 0. A H-bridge cascaded multilevel converter with s separate DC sources is shown in Figure 2.6. A staircase sinusoidal waveform can be generated by combining specified output levels, which is shown in Figure 2.7. The number of output phase voltage levels m in a cascade converter with s separate DC sources is m □ 2s □1. Load balance control for each H-bridge and each DC source can be acquired by rotating the switching angles to the H-bridges [2].

The advantages for cascaded multilevel H-bridge converter are the following:

(1) The series structure allows a scalable, modularized circuit layout and packaging due to the identical structure of each H-bridge.

(2) No extra clamping diodes or voltage balancing capacitors is necessary.

(3) Switching redundancy for inner voltage levels is possible because the phase voltage is the sum of each bridge's output.

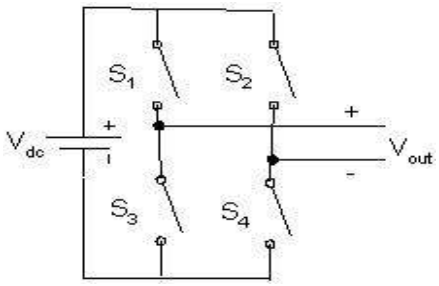

Figure 2.4: Two-phase capacitor-clamped multilevel converter

Cascaded H-bridge Converter:

A cascaded H-bridge converter is several H-bridges in series configuration [2], [7], [8], [12]. A single H-

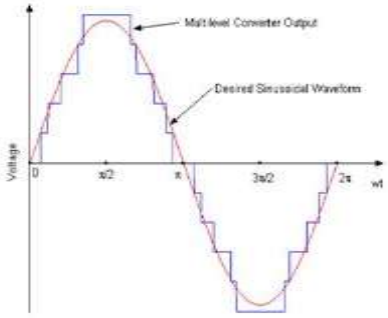

Figure 2.6: H-bridge cascaded multilevel converter with s separate DC sources

The disadvantage for cascaded multilevel H-bridge converter is the following:

(1) Needs separate DC sources;

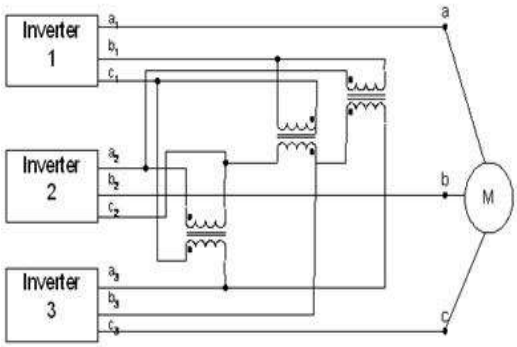

Figure 2.7: Staircase sinusoidal waveform generated by H-bridge cascaded multilevel converter

Another kind of cascaded multilevel converters with transformers using standard three-phase bi-level converters has recently been proposed [8]. The circuit is shown in Figure 2.8. The converter uses output transformers to add different

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voltages. In order for the converter output voltages to be added up, the outputs of the three converters need to be synchronized with a separation of 120□ between each phase. For example, obtaining a three-level voltage between outputs a and b, the output voltage can be synthesized by $V_{ab} = V_{a1\text{-}b1}+V_{b1\text{-}a2}+V_{a2\text{-}b2}$. An isolated transformer is used to provide voltage boost. With three converters synchronized, the voltages $V_{a1\text{-}b1}$, $V_{b1\text{-}a2}$, $V_{a2\text{-}b2}$, are all in phase; thus, the output level can be tripled [13].

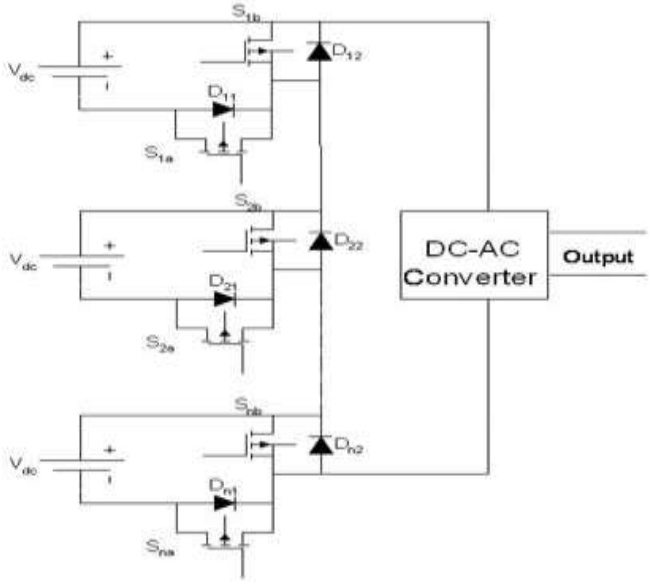

Figure 2.8: Cascaded multilevel converter with transformers using standard three-phase bi-level converters

The advantage for the cascaded multilevel converters with transformers using standard three-phase bi-level converters is the three converters are identical. So control would be simple. The topology has two disadvantages. The first is the three converters need separate DC sources; the second is it needs a transformer to add up the output voltages.

2.2.4. Cascaded DC Sources Multilevel Converter and Cascaded Transformers Multilevel Converter

There are other kinds of topologies for multilevel converters.

Figure 2.9 is a cascaded DC sources multilevel converter [16]. The states of the switches S_{ia} and S_{ib} decide if the level is to be connected into the circuit. If S_{ia}isON, $S_{ib}$is OFF: this level is connected into the circuit. If S_{ia}isOFF, $S_{ib}$is ON: this level is disconnected from the circuit. This topology is proposed for fuel cell applications. The output voltage of a fuel cell will decrease when the load increases, therefore control of the fuel cell number connected into the circuit can keep the output voltage constant [16].

The advantage for the topology is the system is simple and the converters could be identical. Therefore the control would be simple. Another advantage is that a single common DC voltage source is used. The disadvantage is that the system needs output transformers to add up the output voltages

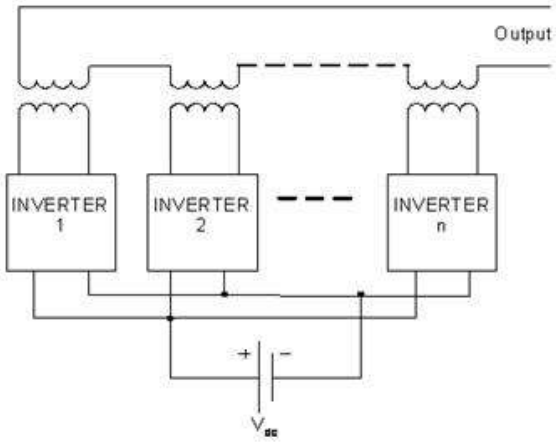

Figure 2.9: Topology of cascaded DC sources multilevel converters

The advantage of the topology is it can reduce the input voltage ripple for the output converter. Another topology for multilevel converters is the cascaded transformer multilevel converter [15], which is shown in Figure 2.10. This opology uses a single DC source and several transformers to generate high voltage output. The topology is similar to topology of the cascaded H-bridge multilevel converters [15].

3. CONCLUSION

In this paper, at the first, a new reduced components SCC topology was presented which has boost capability remarkably and also can pass the reverse current for inductive loads through existing power switches. The voltage of all capacitors in this structure is balanced by binary asymmetrical algorithm. Next, a new sub-multilevel structure based on suggested SCC was proposed which can generate all of the voltage levels at the output (even and odd). In this case, the conventional output H-bridge cell used to convert the polarity of SCC units, has been removed, therefore number of required IGBTs and other involved components, are decreased. After that, an optimizing operation was presented which could obvious the number of required capacitors in each of SCC units that participate in the cascade sub-multilevel inverter (CSMLI) to generate maximum number of output voltage levels with less number of elements. Moreover, comprehensive comparisons were given which prove the differences between improved symmetric and asymmetric CSMLIs in contrast to some of recently presented topologies in variety aspects. Finally, to confirm the performance and effectiveness of proposed CSMLI, several simulation and experimental results have been presented

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