INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)

e-ISSN : 2583-1062

Impact Factor : 5.725

www.ijprems.com
editor@ijprems.com

Vol. 03, Issue 07, July 2023, pp : 28-32

OPTIMAL MANUFACTURING METHOD FOR MINIMIZING POWER CONSUMPTION IN COMPUTER CHIPS

Farah Hatem Khorsheed[1]

[1]Electronic Computer Center, University of Diyala, Diyala, Iraq

DOI: https://www.doi.org/10.58257/IJPREMS31765

ABSTRACT

There are multiple methods available for producing computer chips, and each method has its own advantages and disadvantages. To assess these methods, we must take into account the limitations of a particular situation and select the most suitable approach. A prime illustration of this is determining the optimal method for conserving power in devices such as smartphones or tablets. Recent research has revealed that smaller semiconductors require more energy to operate, yet they ultimately consume less power. Conversely, larger semiconductors consume more power as they increase in size. The lowest power consumption is achieved with 45nm NAND gates. This makes it a good choice for devices that need low power consumption, such as smartphones and tablets. Storage can be reduced to reduce the time it takes for data to decay. This reduces the time it takes for data to grow and affects the overall time it takes to traverse the gateway within the device. 45nm technology has the lowest latency between sending and receiving signals, resulting in the shortest overall transmission time..

Keywords: power, chip, gate, VLSI, circuit.

1. INTRODUCTION

Logic gates, when used with Hspice, allow for exploration of how the output varies based on different design methodologies. These electrical components enable the acquisition of logic outputs from one or more inputs. The range of logic gates extends from simple ones to those used in large scale computers [1]. NAND and NOR gates, which are frequently employed, can be combined to form all other gates. Charles Sanders Pierce elucidated in his article the utilization of generic gates like NAND and NOR to create various types of fundamental logic gates [2]. Henry M. Schaeffer was the first to publish this knowledge. For instance, NOR transistors are utilized in more conventional computer systems, while NAND is the predominant storage technology in smartphones and other portable devices.

2. NAND GATES ARE USED FOR DATA ONLY, NOT NOR GATES.

NAND gates are more susceptible to latency due to their higher overall circuit impedance caused by the PMOS connection, while NOR gates have a longer delay time which affects the circuit as a whole. On the other hand, the NAND structure is better suited for circuits that require changing voltage levels due to its lower gate leakage current. Additionally, when using an OR-OR gate, the output scale transistor is different for the "or" path depending on whether it uses PMOS or NMOS transistors.

3. TECHNOLOGY IS UTILIZED FOR THE PRODUCTION OF CHIP TRANSISTORS.

When designing an electronic circuit, the length of a transistor's channel is more crucial than its width. Furthermore, the channel length feature has an impact on the transistor length during simulation [3].

4. DIFFERENT TYPES OF LOGIC GATES AVAILABLE

4.1 OR GATE

The OR gate is a device that enables you to accomplish this task. For example, if you have a light switch that can be turned on using either a light or a power button, having the light switch on the left and the power button on the right will result in turning on both the light and the power when the light switch is activated. However, if the light switch is on the right and the power button is on the left, turning on the power with the power button will turn off the light. The "OR" gate is a device that allows you to combine elements that are either both true or both false. When you input two items into the OR gate, as shown in Figure 1, it only allows one of them to pass through at a time. Therefore, if either A or B is true, the OR gate will also output true [4].

INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)

www.ijprems.com
editor@ijprems.com

Vol. 03, Issue 07, July 2023, pp : 28-32

e-ISSN : 2583-1062

Impact Factor : 5.725

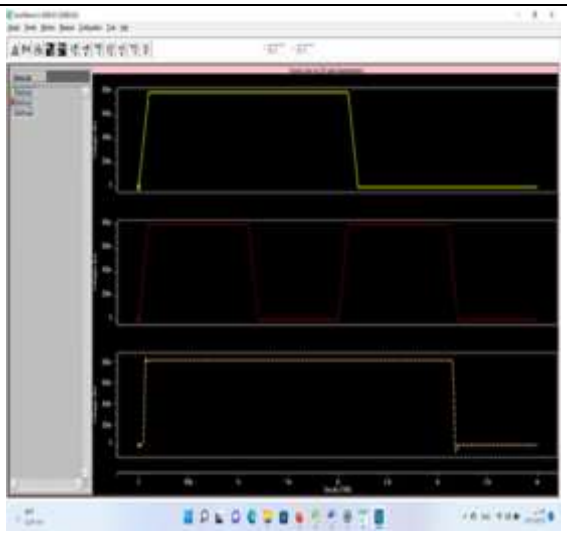

Figure 1: The output waveform of the OR gate is a mixture of the waveforms of the inputs.

4.2 NOR Gate

When the input of a NOR gate is logic level "1", it produces a straight line, but when the input is logic level "0", it produces a dotted line. On the other hand, an OR gate produces a curved line when the input is logic level "0", but produces a straight line when the input is logic level "1". This is illustrated in figure 2 [5].

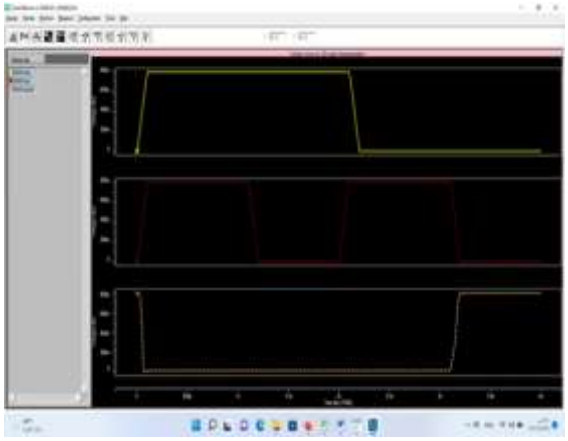

Figure 2: The output waveform of the NOR gate circuit is the opposite of the input waveform.

4.3 AND GATE

The output of a digital logic OR gate will only be "HIGH" if one of its inputs is at a logic level of "1". This means that any high input will result in a high output. The Boolean expression for a numeric OR gate is written as Boolean addition (AB=Q). We can define the numeric operation of the OR gate as follows: "If either A or B is true, then Q is true." This is illustrated in Figure 3. The output of a logic or digital gate will only be "HIGH" if one of its inputs is at a logic level of "1" [6].

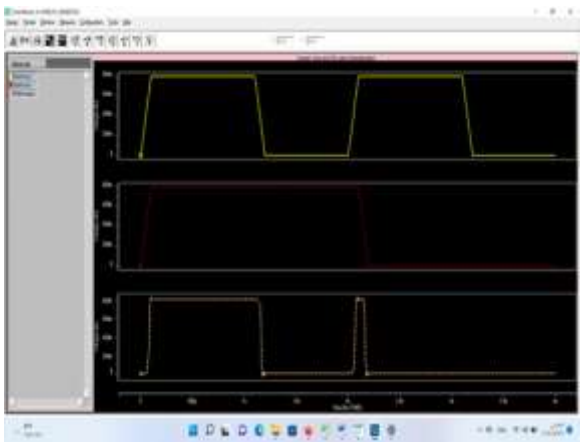

Figure 3: The waveforms for the input and output of the AND gate are illustrated. If both input waves are high, the output will also be high. Conversely, if both input waves are low, the output will be low as well.

INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)

e-ISSN : 2583-1062

Impact Factor : 5.725

www.ijprems.com
editor@ijprems.com

Vol. 03, Issue 07, July 2023, pp : 28-32

4.4 NAND GATE

A NAND gate performs the operation of addition and generates a Boolean outcome only when both inputs are not true. Its symbol is a dot followed by a line with a strikethrough, indicating "not." The output of a NAND gate is true only when both inputs are false [7]. In Figure 4.

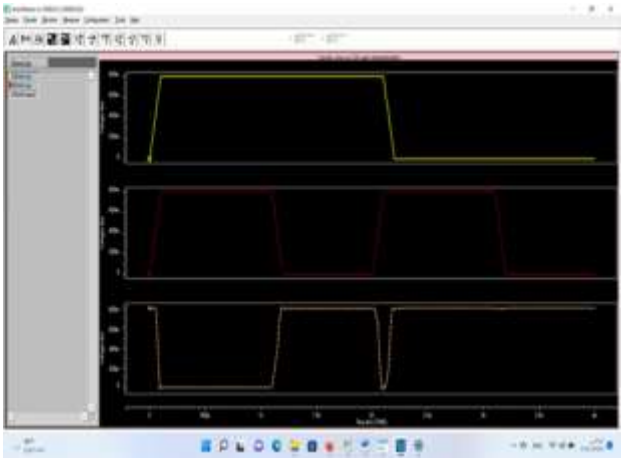

Figure 4: The output waveform generated by the NAND gate circuit is the opposite of the input waveform.

4.5 NOT Gate

A NOT element is a device that receives a 1-level input and produces a 0-level signal. This indicates that the output will consistently be lower than the input, which can be utilized to ensure the functionality of logical expressions. In Figure 5, the NOT valve is depicted as reversing the input signal (reducing it) in order to maintain a consistent output.

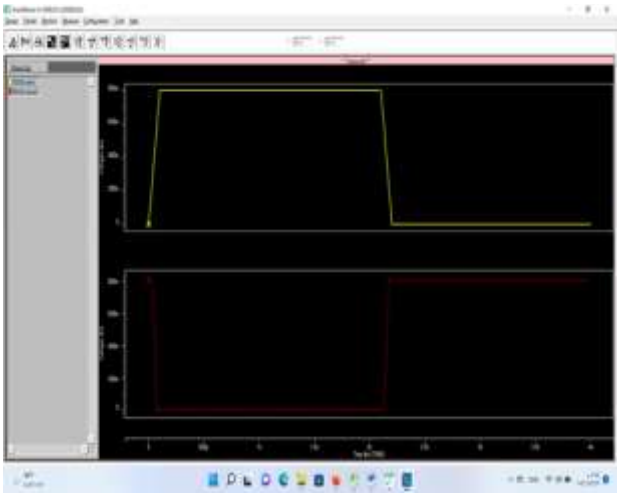

Figure 5: The input and output waveforms of the circuit for the NOT gate.

5. THE SIMULATION AND RESULT OF ALL CIRCUITS WERE COMPLETED.

HSPICE was utilized for modeling different features such as power consumption and latency, and the outcomes of these simulations are displayed in Figure 6-7-8-9. The figure exhibits six circuits, each having distinct power consumption and latency measurements, with the latency measured in picoseconds (ps) and power consumption in milliwatts (mW). The figure highlights the latency and power consumption values for each circuit.

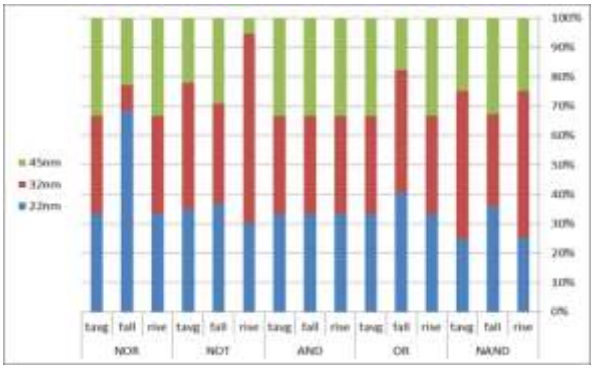

Figure 6: This report includes the increment, decrement, and average time measurements for each gate.

INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)

e-ISSN : 2583-1062

Impact Factor : 5.725

www.ijprems.com
editor@ijprems.com

Vol. 03, Issue 07, July 2023, pp : 28-32

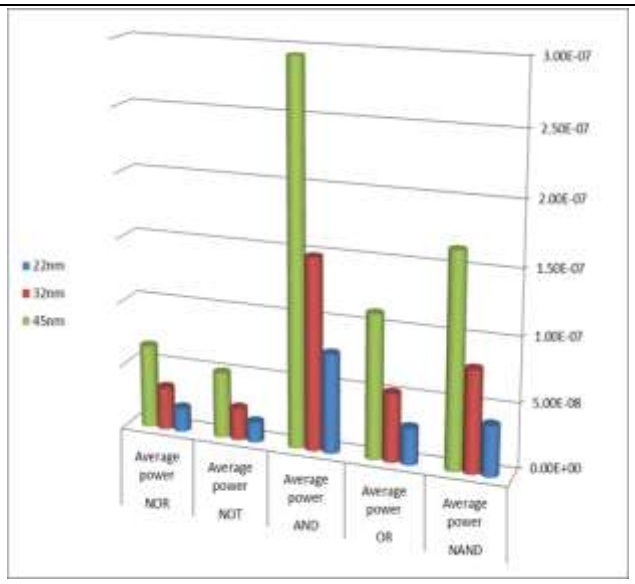

Figure 7: The average performance of Gates utilizing 22nm, 32nm, and 45nm technologies.

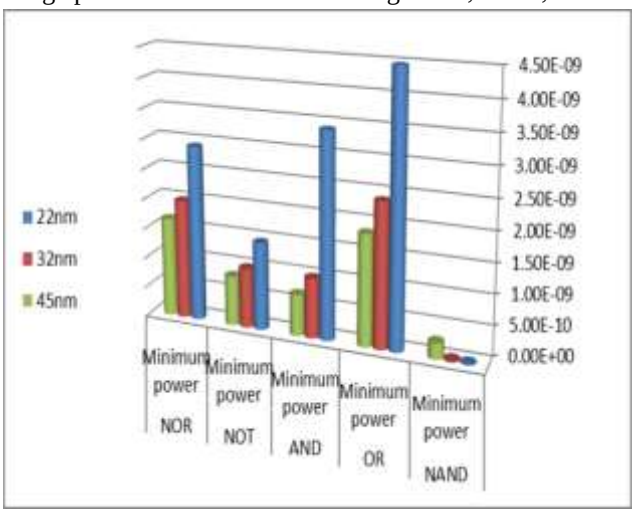

Figure 8: This study analyzes the typical performance of different generations of Gate technology.

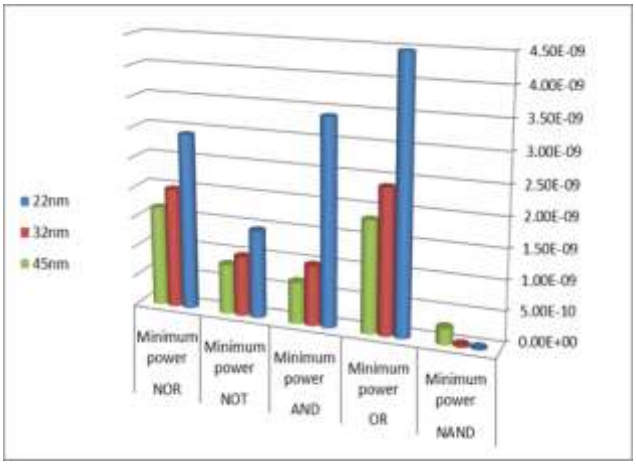

Figure 9: The minimum power level that can be achieved using the latest semiconductor technologies of 22 nm, 32 nm, and 45 nm..

6. CONCULATION

The research discovered that smaller semiconductors consume more energy, but as their size decreases, so does their power consumption. This occurs because small semiconductors require more energy. Opting for 45nm NAND gates is the most efficient approach to energy usage. Hence, it is an excellent choice for energy-saving devices like smartphones and tablets. Utilizing less storage can reduce the deterioration time of data, as well as affect the speed of data accumulation and the overall time it takes for data to pass through the device's gateway. The 45nm technology enables swift transmission by facilitating quick sending and receiving of signals.

7. REFERENCES

[1] Ahmed, W. S., Yaseen, N. A., & Al-Chaabawi, N. J. (2023). Design, Simulation, And Investigation Of Basic Logic Gates By Using Nand Logic Gate. In Nucleation And Atmospheric Aerosols. American Institute Of Physics. Https://Doi.Org/10.1063/5.0119320

[2] Yaseen , N. A. ., Alrawe, W. S. A., & Khudhur , K. A. Khudhur . (2022). Performance Evaluation Of A Low Energy Universal Gate For Vlsi With 16nm Technology. Ntu Journal Of Engineering And Technology, 1(3). Https://Doi.Org/10.56286/Ntujet.V1i3.209

[3] Hosen, K., Islam, M. R., & Liu, K. (2020, December 1). Impact Of Channel Length And Width For Charge Transportation Of Graphene Field Effect Transistor. Chinese Journal Of Chemical Physics, 33(6), 757–763. Https://Doi.Org/10.1063/1674-0068/Cjcp2004055

[4] What Is Logic Gate (And, Or, Xor, Not, Nand, Nor And Xnor)? | Definition From Techtarget. (2020, December 1). Whatis.Com. Https://Www.Techtarget.Com/Whatis/Definition/Logic-Gate-And-Or-Xor-Not-Nand-Nor-And-Xnor

[5] L04: Combinational Logic. (N.D.). L04: Combinational Logic. Https://Computationstructures.Org/Lectures/Combinational/Combinational.Html

[6] Nakarmi, B. (2011, July 1). All-Optical Exclusive-Nor And Exclusive-Or Logic Gate Based On Multi-Input Injection Locking In Single Mode Fabry–Pérot Laser Diode. Optical Engineering, 50(7), 075201. Https://Doi.Org/10.1117/1.3595873

[7] Chek Yee, O., & Soo King, L. (2017, October 22). Nano-Mosfets Implementation Of Different Logic Families Of Two Inputs Nand Gate Transistor Level Circuits: A Simulation Study. Jurnal Teknologi, 79(7). Https://Doi.Org/10.11113/Jt.V79.9947

[8] Storr, W. (2013, September 5). Monostable Multivibrator - The One-Shot Monostable. Basic Electronics Tutorials. Https://Www.Electronics-Tutorials.Ws/Waveforms/Monostable.Html