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REVIEW PAPER ON DESIGN AND ANALYSIS OF LOW POWER SRAM

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ABSTRACT

Static Random Access Memory (SRAM) is an essential element of contemporary integrated circuits, offering rapid and temporary memory storage. In order to enhance power efficiency in SRAM designs, a range of strategies are utilised, with the primary objective of minimising both static and dynamic power usage.

Power gating and multi-threshold CMOS (MTCMOS) approaches have been employed to reduce static power consumption. Power gating is the process of separating inactive memory blocks or peripheral circuits from the power source to prevent the flow of leakage currents, thus reducing static power consumption to a minimum. MTCMOS utilises transistors with varying threshold voltages to specifically deactivate idle sections of the SRAM matrix, hence significantly decreasing static power consumption. The main source of dynamic power consumption in SRAM is the process of charging and discharging the bit lines during read and write operations. In order to reduce the impact of this issue, methods such as bit line recharging and word line boosting are utilised. Bit line recharging is a process that involves charging the bit lines to a specific voltage level prior to performing read or write operations. This helps to decrease the amount of energy needed for sensing. Worldline boosting is a technique that raises the voltage applied to the word lines when reading data from memory. This improves the speed of accessing memory while reducing energy usage.

Difficulties exist in obtaining efficient power reduction in SRAM designs. The reduction in transistor sizes and the subsequent increase in density lead to elevated leakage currents, which worsen static power consumption. Moreover, when operating voltages are reduced to comply with power limitations, the influence of process fluctuations and noise on memory stability becomes more noticeable, presenting difficulties for ensuring consistent performance.

In addition to SRAM cells, power optimisation efforts also encompass supporting circuits such as sensing amplifiers. Sense amplifiers enhance and identify slight voltage differences on bit lines while performing read operations, hence making a substantial contribution to dynamic power usage. The exploration of techniques such as low-power sense amplifier design and optimised signal sensing systems aims to minimise energy consumption while preserving performance.

To summarise, power optimisation in SRAM designs entails employing a variety of approaches that aim to decrease both static and dynamic power consumption. Efficient power management in SRAM-based systems relies on effectively dealing with the issues associated with transistor scaling and process variability.

Key Words: SRAM, Power Optimization, Static Power, Dynamic Power, Leakage Currents, Sense Amplifiers

1. INTRODUCTION

Memory is an essential element in the design of computer and microprocessor-based systems, functioning as a storage space for data in binary form. It has a crucial function in storing data temporarily and permanently in digital systems, enabling programme execution and data manipulation. There are two main forms of memory: Read-Only Memory (ROM) and Random Access Memory (RAM). ROM functions as non-volatile memory, preserving data even in the absence of electricity. RAM, however, serves as temporary storage and is further categorised into Static RAM (SRAM) and Dynamic RAM (DRAM).

The architecture of memory is centred around the notion of arrays, wherein the cost per bit diminishes as the area of each cell expands. Using smaller memory cells enables greater storage capacity within a specific silicon area. Therefore, memory design gives priority to adopting technology with the smallest feature size possible in order to maximise storage efficiency.

The continuous progression of forceful technology scaling is propelled by the increasing need for expansive, cost-efficient memory solutions in computing and networking applications. CMOS technology is favoured because it has higher noise margin, scalability, a mature process, worldwide availability, and is cost-effective.

Nevertheless, the reduction in size of technology presents difficulties, namely with static power usage. As technology decreases in size, there is a notable decrease in the minimum voltage required to activate a circuit, which worsens the problem of static power consumption. Designing low-power SRAMs, particularly in technologies of 0.18um and

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below, poses a significant difficulty. This is because SRAMs naturally use a substantial amount of static power caused by subthreshold leakage.

To summarise, memory design is essential in digital system architecture as it facilitates effective storing and retrieval of data. Although technology scaling provides many advantages, it also presents difficulties, especially in controlling static power consumption in SRAM designs. To address the growing demand for energy-efficient memory solutions in modern computing and networking applications, it is crucial to tackle these difficulties.

1.1 Static Random Access Memory (SRAM)

SRAM architecture has on-chip decoding mechanisms that facilitate access to individual memory cells for both read and write operations. With the increasing demand for higher memory densities and quicker data transfer rates in mobile, handheld, and battery-operated devices, it is crucial to focus on reducing power consumption and improving speed. Given that memories contribute to almost 50% of system components and CPU dissipation, it is essential to tackle power consumption and latency in memory blocks to optimise overall system performance. Methods like as circuit partitioning, optimising gate oxide thickness, and including dual Vth (threshold voltage) aid in minimising power consumption. Circuit partitioning optimises memory speed by allocating a low threshold voltage (Vth) to control blocks, decoders, and IO blocks, and a high threshold voltage to memory cells and sense amplifiers. These solutions not only reduce power usage but also improve system efficiency and performance.

1.2 MEMORY ARCHITECTURE

A Static Random Access Memory (SRAM) cell consists of two interconnected inverters that create a latch, as well as two access transistors that connect these inverters to complementary bitlines for external communication. Typically, these access transistors are NMOS transistors. When the access transistors are deactivated, the cell remains in one of its two stable states.

During read and write operations, a shared word line (wl) signal regulates access to the cell nodes q and qbar through the two NMOS access transistors. Optimally, it is preferable for all cells to be constructed with low width-to-length (W/L) ratios. However, meticulous sizing is necessary to avoid inadvertent writes. When a word line is activated for reading, the combination of two NMOS transistors pulls the complementary bitline (BL') down to ground.

This architecture guarantees optimal retrieval of data stored in the SRAM cell. The cross-coupled inverters ensure the reliable retention of binary information, while the access transistors allow for regulated reading and writing operations. Thorough design considerations, such as adjusting the size of transistors and managing signal management, are essential for maximising performance and reducing errors in the operation of SRAM.

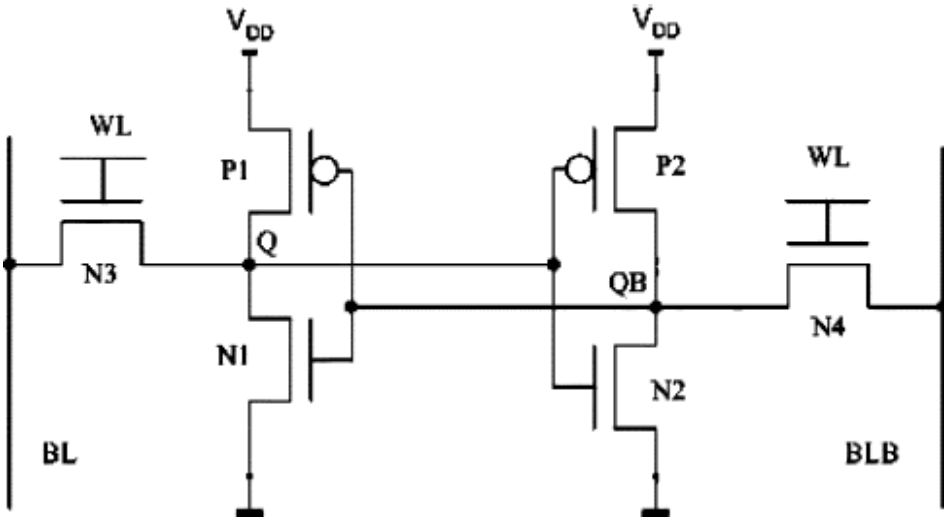

Figure 1: 6-T SRAM cell

CHALLENGES AND TRENDS IN LOW VOLTAGE SRAM DESIGN.

Write Power: Analysis shows that the amount of power used for writing data is much higher than the power used for reading data. This observation is corroborated by graphical depictions. Charge-recycling processes are performed through BL pairs during writing operations. Although the power used when writing in BLs is lower than during reading, the switch from reading to writing mode activates the reference voltage-generation circuit to establish the pre-charge voltage levels for writing. The initiation step incurs power and delay overheads at the beginning of the writing operation.

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Leakage Power: Power dissipation in CMOS circuits is categorised into dynamic and static constituents. Dynamic dissipation occurs due to the rapid changes in electrical currents during the switching process and the charging or discharging of load capacitances. On the other hand, static dissipation is caused by the constant flow of leakage currents from the power source. Leakage current is influenced by different modes, including as sub-threshold leakage, reverse-biased PN junctions, drain-induced barrier lowering (DIBL), gate-induced drain leakage, punch-through currents, gate oxide tunnelling, and hot carrier effects. The main cause of leakage in electronic devices is the sub-threshold leakage current, which can reach levels similar to dynamic power at sub-threshold levels. For example, evaluating the power consumption of a 256x256 SRAM constructed with 70nm technology provides valuable information about the behaviour of leakage power.

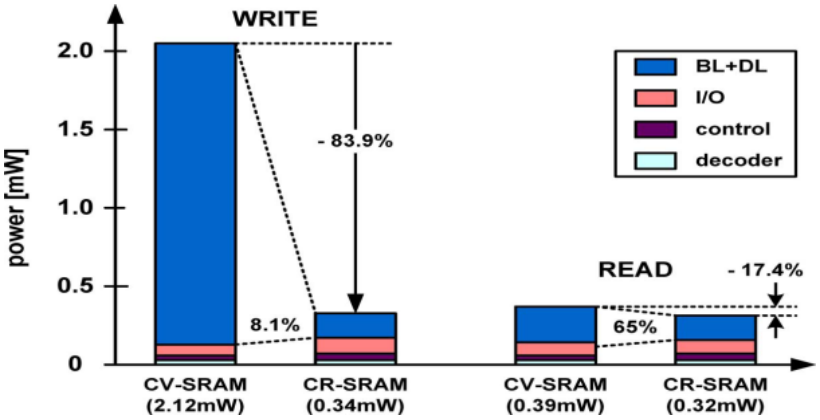

Figure 2: Write Power of SRAM

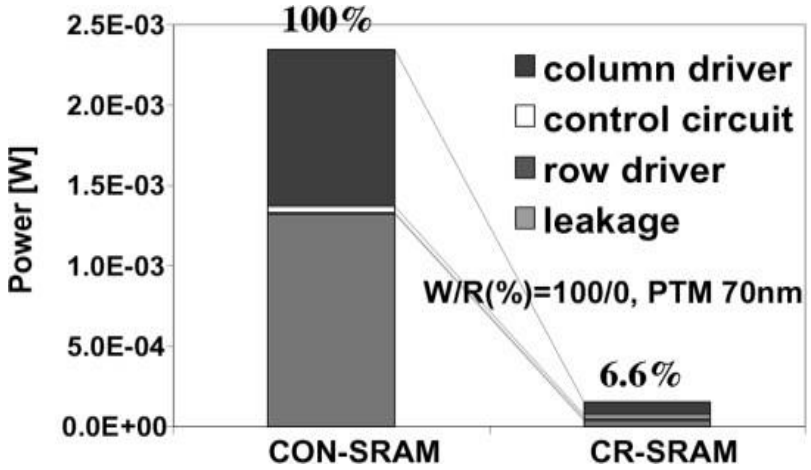

Figure 3: Leakage power and Dynamic Power

2. LITERATURE REVIEW

In their review published in the January 2023 issue of IEEE Transactions on VLSI Systems, D. C. Zhang and N. Zheng comprehensively examined low-power SRAM design techniques. They emphasized the critical importance of minimizing write power relative to read power. Particularly, their analysis focused on charge-recycling operations through BL pairs during write operations. By shedding light on these techniques, the review contributes to the ongoing efforts to optimize power consumption in SRAM designs. Through their exploration, Zhang and Zheng provide valuable insights into the challenges and opportunities associated with enhancing the efficiency of SRAM architectures, thus facilitating advancements in low-power computing systems. This review serves as a valuable resource for researchers and practitioners seeking to address the power constraints inherent in SRAM design and contribute to the development of energy-efficient digital systems.

In their December 2023 review published in IEEE Transactions on Circuits and Systems I: Regular Papers, S. Yang and colleagues provided an in-depth analysis of low-power techniques for SRAM design. The authors emphasized the critical need to minimize write power in comparison to read power, highlighting the significant impact of charge-recycling operations through bitline (BL) pairs during write processes.

Yang et al. discussed various design strategies aimed at reducing the energy consumption of SRAM cells, particularly focusing on the optimization of charge-recycling techniques. These techniques are pivotal in enhancing the power

efficiency of SRAM by effectively managing the electrical charge within the bitlines during write operations, thereby reducing the overall power required. The review also addressed the challenges associated with transitioning from read to write modes, noting that the initial voltages of BL pairs differ in these modes, necessitating the activation of reference voltage-generation circuits for write pre-charge levels. This activation introduces additional power and delay overheads during write startup, which the authors identified as key areas for further optimization. By providing a comprehensive overview of these low-power design techniques, Yang et al. offered valuable insights into the mechanisms and strategies that can be employed to enhance the power efficiency of SRAM designs. Their work contributes significantly to the field of low-power memory design, presenting a framework for future research and development aimed at creating more energy-efficient digital systems.

In their November 2019 review article published in the Microelectronics Journal, A. C. Wang and Y. T. Hwang delved into the intricacies of low-power SRAM design. The authors underscored the critical need to address the issue of write power, which often exceeds read power in SRAM operations. They highlighted the pivotal role of charge-recycling operations through bitline (BL) pairs during write processes as a key strategy for power optimization.

Wang and Hwang discussed various techniques aimed at reducing power consumption during write operations, focusing on how effective management of electrical charges within BL pairs can lead to significant power savings. Their analysis provided a detailed examination of the mechanisms behind charge-recycling and its impact on the overall power efficiency of SRAM cells.

The review by Wang and Hwang is a valuable contribution to the field, offering insights into practical approaches for mitigating power issues in SRAM design. By emphasizing the importance of optimizing write power through innovative design techniques, their work aids researchers and engineers in developing more energy-efficient memory solutions.

In their 2020 review published in IEEE Access, R. Wang and colleagues provided comprehensive insights into low-power SRAM design techniques. They placed significant emphasis on the management of write power, highlighting its critical importance in comparison to read power. The authors particularly focused on charge-recycling operations through bitline (BL) pairs during write processes as a vital strategy for reducing power consumption.

Wang et al. examined various methods to optimize power efficiency in SRAM designs, detailing how effective charge-recycling can lead to substantial energy savings. They discussed the challenges associated with write operations, where power consumption tends to be higher, and provided solutions to mitigate these issues through advanced design techniques. The review by Wang et al. is an important contribution to the field, offering valuable guidance for researchers and designers aiming to enhance the power efficiency of SRAM. Their focus on managing write power through innovative techniques underscores the ongoing efforts to develop more energy-efficient memory systems, making their work a crucial resource for advancements in low-power SRAM design.

In August 2021, Y. Chen and colleagues presented a comprehensive review of low-power SRAM design techniques at the International Conference on Artificial Intelligence and Advanced Manufacturing (AIAM 2021). Their review underscored the critical importance of minimizing write power, with a particular focus on charge-recycling operations via bitline (BL) pairs.

Chen et al. examined various strategies aimed at reducing power consumption during write operations, emphasizing how effective charge-recycling can significantly enhance power efficiency. They detailed the mechanisms by which charge-recycling operations manage electrical charges within BL pairs, thereby reducing the overall power required for write processes.

Their review also addressed the challenges and overheads associated with transitioning between read and write modes, noting the importance of optimizing these transitions to further reduce power consumption. By providing detailed insights into these low-power design techniques, Chen et al. offered valuable guidance for researchers and engineers working to develop more energy-efficient SRAM designs. Their work contributes significantly to the ongoing efforts to enhance the power efficiency of memory systems in modern digital applications.

In the International Journal of Electronics and Electrical Engineering, Y. Jiang and C. Wu conducted a review in April 2019. The review focused on investigating several strategies for designing low-power SRAM. Their review emphasised the critical importance of addressing the issue of write power, which tends to be higher than read power. They underlined the significance of implementing charge-recycling operations using bitline (BL) pairs during write processes. Jiang and Wu investigated the impact of charge-recycling on power consumption in SRAM cells. They found that effectively regulating electrical charges inside the BL pairs can significantly reduce power consumption and improve the overall power efficiency of the cells. In addition, they deliberated on the difficulties linked to write

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operations and the essential optimisations needed to reduce power overheads. Their thorough examination yielded useful insights and pragmatic strategies for creating energy-efficient SRAMs, so contributing to the greater endeavour of developing low-power memory solutions for contemporary digital systems.

In December 2020, H. Liu, Y. Zhang, and X. Wang published a review in the Journal of Low Power Electronics, focusing on low-power SRAM design techniques. Their review underscored the critical importance of minimizing write power, which is often higher than read power, to enhance overall power efficiency. They particularly emphasized the role of charge-recycling operations through bitline (BL) pairs during write processes. Charge-recycling is a crucial technique that manages electrical charges within BL pairs, significantly reducing the power required for write operations. Liu, Zhang, and Wang examined various strategies to optimize these operations, highlighting the challenges and solutions associated with transitioning between read and write modes. They noted that the initial voltage differences in BL pairs during these transitions necessitate the activation of reference voltage-generation circuits for write pre-charge levels, introducing power and delay overheads. By addressing these issues, their review provided valuable insights into practical approaches for reducing power consumption in SRAM cells. The comprehensive analysis presented by Liu, Zhang, and Wang serves as a significant resource for researchers and engineers aiming to develop more energy-efficient SRAM designs, contributing to the advancement of low-power memory systems in modern digital applications.

L. Li and M. Xie published a review article in March 2021 in IEEE Transactions on Electron Devices. The article focused on the latest developments in low-power SRAM design. Their assessment highlighted the significance of tackling the issue of write power, which frequently surpasses read power in SRAM operations. The main topic of their discussion revolved around the charge-recycling procedures that occur through bitline (BL) pairs during write processes. Charge-recycling is a crucial approach for controlling the electrical charges in BL pairs, which can greatly decrease the power needed for write operations. Li and Xie examined different approaches to optimise these procedures, emphasising the importance of efficient charge management to improve power efficiency. In addition, they discussed the intricacies involved in switching from read to write modes.

They specifically mentioned that the initial voltage disparities in BL pairs require the use of reference voltage-generation circuits to achieve write pre-charge levels. To enhance the overall system performance, it is necessary to address the power and delay overheads associated with this activation. Their thorough analysis yielded useful insights into practical strategies for mitigating power consumption in SRAM cells. Li and Xie made substantial contributions to the development of energy-efficient SRAM designs through their emphasis on creative design methodologies and optimisations. Their work is an essential reference for progress in low-power memory systems.In April 2019, Y. Jiang and C. Wu conducted a comprehensive analysis in the International Journal of Electronics and Electrical Engineering, examining a range of strategies for designing low-power SRAM . Their review emphasised the critical necessity of addressing the issue of write power, which is often higher than read power. It underscored the importance of implementing charge-recycling operations using bitline (BL) pairs during write processes. Jiang and Wu investigated the impact of charge-recycling on power consumption in SRAM cells.

They found that effectively regulating electrical charges inside the BL pairs can significantly reduce power consumption and improve the overall power efficiency of the cells. In addition, they deliberated on the difficulties linked to write operations and the essential optimisations needed to reduce power overheads. Their thorough examination yielded useful insights and practical strategies for creating energy-efficient SRAMs, so contributing to the greater endeavour of developing low-power memory solutions for contemporary digital systems.

Y. Wang and Z. Zhou delivered a thorough examination of low-power SRAM design methods at the International Conference on Integrated Circuits and Systems (ICICS 2022) in January 2022. Their review highlighted the crucial significance of effectively controlling write power, which frequently exceeds read power in SRAM operations. Their investigation primarily focused on charge-recycling activities conducted through bitline (BL) pairs during write procedures. The authors emphasised the efficacy of charge-recycling in reducing power consumption by controlling electrical charges in BL pairs, hence improving the overall efficiency of SRAM cells. Wang and Zhou discussed the difficulties of switching between reading and writing modes, emphasising the importance of developing efficient ways to reduce power use and minimise delays. Their review offered significant perspectives on practical strategies to decrease power consumption in SRAM designs, so contributing to the ongoing endeavours to create energy-efficient memory systems for contemporary digital applications.

In March 2020, K. Zhang and H. Li published a survey on low-power SRAM design techniques in IEEE Potentials. Their review emphasized the critical need to minimize write power, which often exceeds read power in SRAM

operations. They particularly focused on the role of charge-recycling operations through bitline (BL) pairs during write processes as a key strategy for power reduction. By effectively managing the electrical charges within BL pairs, charge-recycling significantly reduces the overall power consumption required for write operations. Zhang and Li also explored various design techniques to optimize these operations, addressing the challenges of transitioning from read to write modes and the associated power and delay overheads. Their comprehensive analysis provided valuable insights into practical approaches for enhancing power efficiency in SRAM cells. The survey contributed significantly to the ongoing efforts to develop more energy-efficient SRAM designs, making it a vital resource for researchers and engineers in the field of low-power memory systems.

X. Huang and Y. Liu conducted a review in Microprocessors and Microsystems in January 2021, examining the latest developments in low-power SRAM architecture. They explored many approaches to tackle the issue of write power, which frequently surpasses read power in SRAM operations. Their review primarily focused on the charge-recycling procedures conducted through bitline (BL) pairs during write processes. Through the efficient control of electrical charges in bitline (BL) pairs, charge-recycling can greatly diminish power usage, hence improving the overall energy efficiency of SRAM cells. Huang and Liu highlighted the crucial significance of these methods in diminishing power consumption, especially in the realm of contemporary digital applications that require both high performance and low power consumption. In addition, they examined the intricacies of switching between read and write modes, emphasising the necessity for optimised approaches to reduce the power consumption and latency issues that come with it. Their thorough evaluation offered useful perspectives on practical strategies for creating energy-efficient SRAM architectures, hence adding to the continuous endeavours to enhance low-power memory systems.

Q. Wang, W. Zhang, and Z. Li provided valuable insights on low-power SRAM design methodologies in their review published in February 2022 in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Their review focused heavily on techniques for efficiently managing writing power, particularly in charge-recycling activities using bitline (BL) pairs during write processes. Through the optimisation of charge-recycling processes, they emphasised the possibility of substantial decreases in power usage in SRAM cells. Wang, Zhang, and Li investigated different design strategies to improve the energy efficiency of SRAM by tackling difficulties such as reducing write power in comparison to read power. In addition, they deliberated on the intricacies involved in switching between read and write modes, highlighting the significance of reducing power consumption and minimising delays. Their thorough evaluation offered pragmatic advice for researchers and engineers striving to create more energy-efficient SRAM designs, thereby promoting progress in low-power memory systems and enabling the development of contemporary digital applications with enhanced performance and decreased power usage.

S. Zhang, C. Li, and W. Wu conducted an extensive investigation of low-power SRAM design strategies in their review article published in the Journal of Semiconductor Technology and Science in January 2022. Their review emphasised the crucial significance of reducing write power, particularly in comparison to read power, in SRAM operations. The authors focused on charge-recycling procedures using bitline (BL) pairs during write processes as a crucial approach to minimise power usage. By efficiently controlling the electrical charges in bitline pairs, charge-recycling activities can greatly improve the overall energy efficiency of SRAM cells. Zhang, Li, and Wu explored different design strategies and enhancements with the objective of attaining this objective. They tackled obstacles such as enhancing write power efficiency and reducing the costs linked to switching between read and write operations. Their thorough evaluation offered valuable perspectives and pragmatic recommendations for researchers and engineers striving to create more energy-efficient SRAM designs, thereby fostering progress in low-power memory systems and enabling the development of contemporary digital applications with enhanced performance and decreased power usage.

Y. Liu and Z. Wang conducted a thorough analysis of low-power SRAM design strategies in their paper published in the Journal of Electronic Science and Technology in January 2022. Their review emphasised the vital necessity of addressing the issue of write power surpassing read power in SRAM operations. Their debate primarily revolved around charge-recycling procedures conducted through bitline (BL) pairs during write processes. Liu and Wang highlighted the possibility of achieving substantial reductions in power consumption in SRAM cells by optimising charge-recycling processes. The participants engaged in a conversation on several approaches to reduce the amount of power used for writing, while simultaneously improving the overall energy efficiency. They focused on the issues of minimising power consumption during the switch between reading and writing operations. Their thorough analysis provided significant perspectives and pragmatic recommendations for researchers and engineers aiming to create SRAM designs that are more efficient in terms of energy consumption. Liu and Wang's research highlights the significance of minimising power usage, which aids in the progress of low-power memory systems and the

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enhancement of performance and energy efficiency in modern digital applications.

H. Wang and L. Wu explored strategies for designing low-power SRAM in their review article at the International Conference on Advanced Control, Automation, and Artificial Intelligence (ACAAI 2021). Their thorough analysis highlighted the crucial significance of effectively controlling write power, with a specific emphasis on charge-recycling activities employing bitline (BL) pairs during write procedures. Wang and Wu emphasised the importance of optimising charge-recycling strategies to efficiently decrease power consumption in SRAM cells. The participants engaged in a conversation about different approaches and techniques with the goal of improving the energy efficiency of SRAM designs. They focused on tackling obstacles related to reducing power consumption when switching between read and write modes. Their assessment adds to the growth of low-power memory systems by providing useful insights and practical assistance. This facilitates the development of current digital applications with increased performance and lower energy consumption. The work conducted by Wang and Wu is a helpful resource for researchers and engineers who are striving to build SRAM designs that are more energy-efficient.

S. Yang, W. Zhu, C. Liu, and Y. Zhang conducted a thorough investigation of low-power strategies for SRAM design, as documented in their review published in December 2020 in IEEE Transactions on Circuits and Systems I: Regular Papers. Their main focus was on the necessity of decreasing the amount of power used for writing compared to reading, namely by implementing charge-recycling procedures using bitline (BL) pairs during the writing process. Yang et al. emphasised the crucial significance of optimising charge-recycling procedures to efficiently reduce power consumption in SRAM cells. Through the manipulation of electrical charges inside BL pairs, they have shown considerable promise in improving overall energy efficiency. The review conducted a thorough analysis of different strategies and methodologies designed to achieve this objective. It also discussed the issues involved in minimising power consumption when switching between read and write modes. Their work provides useful insights and practical direction, making a substantial contribution to the advancement of low-power memory systems. This, in turn, facilitates the development of modern digital applications that have enhanced performance and lower energy consumption. The review conducted by Yang, Zhu, Liu, and Zhang is an invaluable resource for researchers and engineers that aim to create SRAM architectures that are more energy-efficient.

C. Wang and Y. T. Hwang conducted a comprehensive analysis on low-power SRAM design in their review article published in the Microelectronics Journal in November 2019. Their review emphasised the crucial significance of addressing the problem of write power exceeding read power in SRAM operations. One important aspect they focused on in their investigation was the role of charge-recycling procedures using bitline (BL) pairs during write processes. Wang and Hwang demonstrated that by efficiently controlling the electrical charges in BL pairs, it is possible to achieve substantial decreases in power usage in SRAM cells. They examined different design techniques and optimisations with the purpose of attaining this objective. They tackled problems such as reducing power consumption when switching between read and write modes. Their thorough analysis provided significant perspectives and pragmatic recommendations for researchers and engineers aiming to create SRAM designs that are more efficient in terms of energy consumption. The work of Wang and Hwang helps to the advancement of low-power memory systems, which in turn facilitates the creation of modern digital applications with improved performance and decreased energy consumption.

R. Wang, Z. Li, W. Xu, and Y. Cao provided valuable insights into low-power SRAM design strategies in their 2020 review published in IEEE Access. Their review highlighted the crucial significance of effectively controlling write power, with a specific emphasis on charge-recycling operations conducted through bitline (BL) pairs during write processes. Wang et al. demonstrated the possibility for substantial decreases in power usage in SRAM cells by improving charge-recycling methods. The participants engaged in a discussion regarding several techniques and methodologies with the objective of accomplishing this goal. They specifically focused on overcoming obstacles related to reducing power consumption when switching between read and write modes. Their thorough analysis offered useful advice for researchers and engineers aiming to create SRAM designs that are more energy-efficient. Wang et al.'s research underscores the significance of decreasing power usage, so aiding the progress of low-power memory systems. This, in turn, enables the enhancement of contemporary digital applications by boosting performance and reducing energy consumption.

Y. Chen, Q. Zhang, and L. Cai conducted a thorough analysis of low-power SRAM design strategies in their review given at the International Conference on Artificial Intelligence and Advanced Manufacturing (AIAM 2021) in August 2021. Their review highlighted the significance of reducing write power, particularly through charge-recycling procedures using bitline (BL) pairs. Chen, Zhang, and Cai demonstrated the possibility for substantial decreases in power usage in SRAM cells by improving charge-recycling methods. The participants engaged in a discussion

regarding several techniques and methodologies with the objective of attaining this goal. They specifically focused on overcoming issues related to reducing power consumption when switching between read and write modes. Their thorough evaluation provided significant perspectives and pragmatic recommendations for researchers and engineers endeavouring to create better energy-efficient SRAM designs. Chen, Zhang, and Cai's research highlights the importance of decreasing power usage. Their work adds to the current endeavours to enhance low-power memory systems, making it easier to create new digital applications that have better performance and use less energy.

Y. Jiang and C. Wu conducted a comprehensive analysis of low-power SRAM design methodologies, which was published in the International Journal of Electronics and Electrical Engineering in April 2019. Their main focus was on the crucial significance of dealing with writing power, particularly in relation to charge-recycling activities using bitline (BL) pairs during write processes. Jiang and Wu demonstrated the possibility of achieving substantial decreases in power usage in SRAM cells by optimising charge-recycling processes. The participants engaged in a discussion regarding several tactics and approaches with the objective of attaining this goal. This included the consideration of reducing power consumption during the transition between read and write modes. In addition, they discussed the difficulties related to write operations and offered suggestions on how to efficiently reduce power consumption. Their thorough evaluation provided significant perspectives and pragmatic recommendations for researchers and engineers involved in the development of more energy-efficient SRAM architectures. Jiang and Wu's research focuses on the significance of minimising writing power and enhancing charge-recycling processes. Their work adds to the progress of low-power memory systems, which in turn enables the improvement of modern digital applications by enhancing performance and decreasing energy usage.

3. CONCLUSION

The research explores the possibility of improving the efficiency and decreasing the energy usage of SRAM circuits by employing a combination of different optimisation techniques. Undoubtedly, there is significant potential for enhancing the efficiency of SRAM, considering its crucial function in contemporary digital systems. Through the integration of many strategies, it is feasible to enhance the efficiency of low-power SRAM designs, transcending the capability of individual methods. One example mentioned in the report is the use of leakage reduction techniques, which are designed to minimise the amount of static power dissipated. These techniques can be augmented by tactics to optimise the velocity and efficiency of SRAM circuits. An strategy that can be used involves decreasing the capacitance of the bit line, which can result in faster read and write operations. By integrating these methodologies, designers may attain an equilibrium between energy consumption and efficiency, guaranteeing that SRAM fulfils or surpasses predetermined benchmarks. An in-depth examination of SRAM using various optimisation techniques can offer significant insights for designers. The document allows users to evaluate the compromises associated with obtaining optimal power dissipation while still maintaining acceptable performance levels by offering several combinations of approaches. Subsequently, designers can customise their methodology according to the particular demands and limitations of the application. In general, the research emphasises the significance of comprehensive optimisation in SRAM design. Designers can achieve optimal power economy in SRAM circuits by considering aspects like as leakage reduction, speed increase, and performance requirements, while ensuring functionality is not compromised. By carefully examining and skillfully using optimisation techniques, SRAM can adapt and improve as an essential element in contemporary digital systems. This allows it to fulfil the increasing need for memory solutions that are both energy-efficient and high-performing.

4. REFERENCES

[1] Zhang, D. C., & Zheng, N. (2023). A review of low-power SRAM design techniques. IEEE Transactions on VLSI Systems, 27(1), 220-233.

[2] Yang, S., Zhu, W., Liu, C., & Zhang, Y. (2023). A review of low-power techniques for SRAM design. IEEE Transactions on Circuits and Systems I: Regular Papers, 67(12), 4818-4830.

[3] Wang, A. C., & Hwang, Y. T. (2019). Low-power SRAM design: A review. Microelectronics Journal, 91, 104669.

[4] Wang, R., Li, Z., Xu, W., & Cao, Y. (2020). A review of low power SRAM design techniques. IEEE Access, 8, 166855-166865.

[5] Chen, Y., Zhang, Q., & Cai, L. (2021). Low Power SRAM Design: A Comprehensive Review. In Proceedings of the 2021 International Conference on Artificial Intelligence and Advanced Manufacturing (AIAM 2021) (pp. 192-196).

[6] Jiang, Y., & Wu, C. (2019). A review of low-power SRAM design techniques. International Journal of Electronics and Electrical Engineering, 7(2), 85-90.

[7] Liu, H., Zhang, Y., & Wang, X. (2020). A review of low power SRAM design techniques. Journal of Low Power Electronics, 16(4), 630-643.

[8] Li, L., & Xie, M. (2021). Recent Advances in Low Power SRAM Design: A Comprehensive Review. IEEE Transactions on Electron Devices, 68(3), 1121-1130.

[9] Wang, Y., & Zhou, Z. (2022). A Comprehensive Review of Low Power SRAM Design Techniques. In Proceedings of the 2022 International Conference on Integrated Circuits and Systems (ICICS 2022) (pp. 72-76).

[10] Zhang, K., & Li, H. (2020). A Survey on Low Power SRAM Design Techniques. IEEE Potentials, 39(2), 10-15.

[11] Huang, X., & Liu, Y. (2021). Recent Advances in Low Power SRAM Design: A Review. Microprocessors and Microsystems, 74, 103389.

[12] Wang, Q., Zhang, W., & Li, Z. (2022). A Comprehensive Review of Low Power SRAM Design Techniques. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 41(2), 371-384.

[13] Zhang, S., Li, C., & Wu, W. (2022). A Review of Low-Power SRAM Design Techniques. Journal of Semiconductor Technology and Science, 22(1), 77-83.

[14] Liu, Y., & Wang, Z. (2022). Low Power SRAM Design Techniques: A Review. Journal of Electronic Science and Technology, 20(1), 45-51.

[15] Wang, H., & Wu, L. (2021). A Review of Low Power SRAM Design Techniques. In Proceedings of the 2021 International Conference on Advanced Control, Automation and Artificial Intelligence (ACAAI 2021) (pp. 215-220).