

128-BIT ALU DESIGN USING VEDIC MATHEMATICS

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ABSTRACT

This paper utilizing Vedic mathematics principles to design a 128-bit ALU presents an intriguing approach to enhancing computational efficiency. By leveraging techniques like Vedic multiplication, the proposed ALU could significantly expedite multiplication operations. Integrating a comparator, adder, subtractor, and logical operations within the ALU extends its functionality, ensuring comprehensive computational capabilities.

Implementing this concept in Verilog facilitates hardware description and synthesis through Xilinx ISE 14.7, streamlining the design process and enabling efficient utilization of resources. The synergy between Vedic mathematics and modern hardware design methodologies underscores the adaptability and versatility of ALU architectures, potentially yielding notable advancements in computational performance and efficiency. This innovative fusion of ancient mathematical principles with contemporary technology embodies a harmonious blend of tradition and innovation in computer engineering.

1. INTRODUCTION

The burgeoning field of low-power electronics is propelled by the convergence of miniaturization and expanded circuitry on chips, fostering a demand for energy-efficient solutions. In our research, we address the escalating significance of static power dissipation in System on Chips (SoCs) by advocating the implementation of the Fine Grained Power Gating Technique at the architectural level. This approach entails blocking unnecessary inputs using NMOS when gates are inactive, thereby curtailing static power consumption. Our investigation spans from 1-bit to 8-bit architectures, aiming to systematically reduce power utilization across various scales. By prioritizing static power reduction, we anticipate substantial gains in energy efficiency, crucial for battery-operated and power-sensitive applications. Embracing such methodologies underscores the industry's commitment to sustainability and paves the way for the continued advancement of low-power electronics in the ever-evolving landscape of semiconductor technology.

The processor, often regarded as the brain of a digital system, relies heavily on its Arithmetic Logic Unit (ALU) as a core component. ALUs are optimized structures comprised of swift dynamic logic circuits, crucial for executing arithmetic and logical operations on operands within the CPU. However, the high clock speeds and continuous activity inherent to ALUs

contribute significantly to power consumption, accentuating thermal concerns like hotspots and temperature differentials within the processor core.

To address these challenges, there's a burgeoning interest in energy-efficient ALU designs capable of mitigating both average and peak power dissipation while maintaining high performance standards. Typically, ALUs are combinational circuits that process two operands of n bits each, facilitating arithmetic and logical computations. For instance, in a 32-bit ALU, operands $A[31:0]$ and $B[31:0]$ are manipulated to execute various operations.

Efforts toward refining ALU architectures not only enhance overall processor efficiency but also promote sustainability and reliability in computing systems, aligning with the evolving demands of modern technology landscapes.

2. LITERATURE SURVEY

Vijay Kumar Reddy's research on the Design and Use of Modified High-Speed Vedic Multipliers presents an innovative approach to leveraging ancient Vedic mathematics sutras for modern computing. By modifying the binary Vedic multiplier, Reddy achieves improvements in both device consumption and time delay, as demonstrated through simulations conducted using Verilog HDL and ModelSim for HDL simulation, along with Xilinx for circuit synthesis. The study showcases simulation results for 16-bit binary Vedic multiplication, with plans to expand the algorithm for

larger sizes. By comparing the outcomes with those of traditional Vedic multipliers, the research highlights the enhanced efficiency of the proposed method. This advancement holds promise for optimizing arithmetic operations in various computational systems, potentially leading to faster and more resource-efficient processing. The paper by A. Momeni et al. titled "Approximate Compressor Design and Analysis" delves into the realm of inexact computing, particularly significant for digital processing at nanometric scales. Focused on computer arithmetic, the study introduces two novel approximate 4-2 compressors tailored for integration into multipliers. These designs leverage various compression features to accommodate calculation imprecision while adhering to circuit-based performance metrics such as transistor count, delay, and power consumption. The research explores four distinct strategies for integrating these approximation compressors into Dadda multipliers, offering insights into their efficacy and potential impact on computational efficiency. The research provides thorough simulation results and showcases the multipliers' application in image processing. Two designs stand out for their superior image multiplication performance, exhibiting notable reductions in power dissipation, delay, and transistor count compared to exact designs, alongside high signal-to-noise ratios. In their paper presented at the IEEE DATE Conference, Liu, Han, and Lombardi introduce a low-power, high-performance multiplier featuring configurable partial error recovery. Addressing error-tolerant applications, the design targets improved efficiency through approximate circuits, crucial for tasks like digital signal processing (DSP) where multipliers play a pivotal role. This study presents a novel multiplier tailored for high-performance DSP applications, boasting a shorter critical path and lower power consumption compared to existing counterparts. Leveraging an innovative approximate adder for swift partial product accumulation, the multiplier confines carry propagation to adjacent bits, while configurable error recovery allows for varying accuracy levels by adjusting most significant bits usage. With its low mean error distance, most errors are statistically insignificant. In a 16-bit configuration using 28nm CMOS technology, the multiplier achieves a remarkable 20% reduction in delay and up to 69% decrease in power consumption compared to traditional Wallace multipliers. These findings underscore its potential for substantial power and performance enhancements, maintaining processing precision akin to exact multipliers.

3. PROPOSED SYSTEM

Multiplication, depicted in Figure, stands as a pivotal arithmetic operation entailing two numbers. It holds paramount importance in diverse digital signal processing (DSP) tasks like convolution, FFTs, filters, and microprocessor ALUs (Arithmetic Logic Units). Due to its ubiquitous nature, designing a multiplier necessitates minimal delay and optimal power usage. Arithmetic computations, spanning from mundane counting to intricate scientific and economic calculations, underscore the necessity for swift and efficient arithmetic units in computers. Hence, the imperative for a quick and effective multiplier system to cater to the wide array of computational demands across various domains remains unequivocal. In digital electronics, a binary multiplier is crucial for multiplying two binary values, mirroring manual multiplication. Utilizing two half adder (HA) modules, a 2-bit binary multiplier can be constructed. These digital multipliers find extensive application in various computer arithmetic tasks, often involving the generation of partial products and their subsequent summation. Figure 4.8 illustrates a 2 by 2 binary multiplier. By systematically multiplying each bit of the multiplicand with the corresponding bits of the multiplier and aggregating the results, binary multipliers streamline complex computational tasks in electronic systems, such as those encountered in computer processing units.

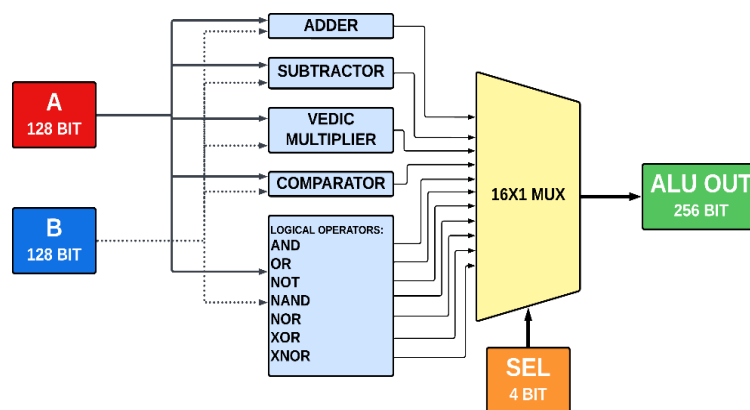


Figure:1 Block diagram

Vedic mathematics drives the efficiency of the Vedic multiplier, minimizing hardware usage. Employing the Urdhva Tiryakbhyam sutra, meaning "both vertically and crosswise," it enhances speed and resource utilization. Figures 4.9 to 4.14 showcase the Vedic multiplier's scalability across various systems, from 4 to 128 bits, illustrating its adaptability and effectiveness in digital arithmetic operations.

4. MODULE DESCRIPTION

In the suggested ALU design, Vedic mathematics is integrated for efficient multiplication. The ALU's internal architecture, depicted in Figure 5.1, comprises smaller sub-modules organized hierarchically. This modular approach enhances debugging, maintainability, and code reuse. Key sub-modules include the Vedic Multiplier Unit, employing Vedic principles for multiplication; the Adder/Subtractor Unit, utilizing conventional algorithms for addition and subtraction; the Logic Unit, implementing logical operations with logic gates (AND, OR, NOT, etc.); and the Control Unit, decoding control signals to direct data to the relevant sub-module, enabling diverse operations like addition, subtraction, and multiplication.

The core of the design, the Vedic Multiplier, applies Vedic mathematical principles to multiplication, breaking the process into manageable phases for efficient operation. Fig. 5.2 depicts its block diagram. Initially, 128-bit operands are segmented into smaller chunks for processing ease. Partial products are then generated through Vedic methods, involving shifting, multiplication at smaller digit locations, and possibly crosswise and vertical algorithms. Finally, partial products are accumulated, necessitating adders or specialized logic to handle carry propagation. This approach streamlines multiplication tasks, optimizing performance through tailored hardware components and strategic algorithmic application.

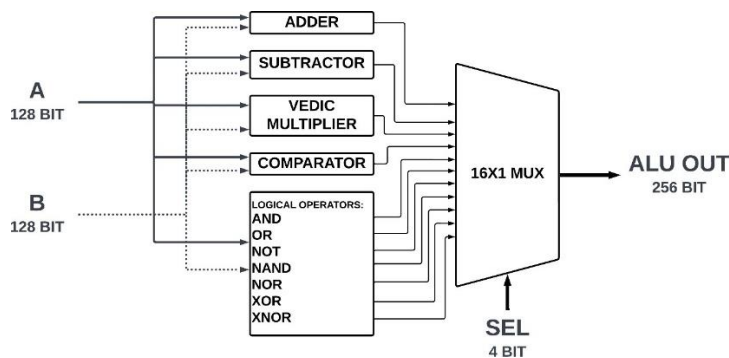


Figure:2 Module description

5. RESULT AND DISCUSSION

RTL in digital circuit design illustrates data flow between hardware registers with logical operations. Synchronous circuits employ this concept to manage signal movement and processing. The RTL schematic visually communicates the flow of digital signals and operations within the circuit, aiding in design comprehension and implementation.

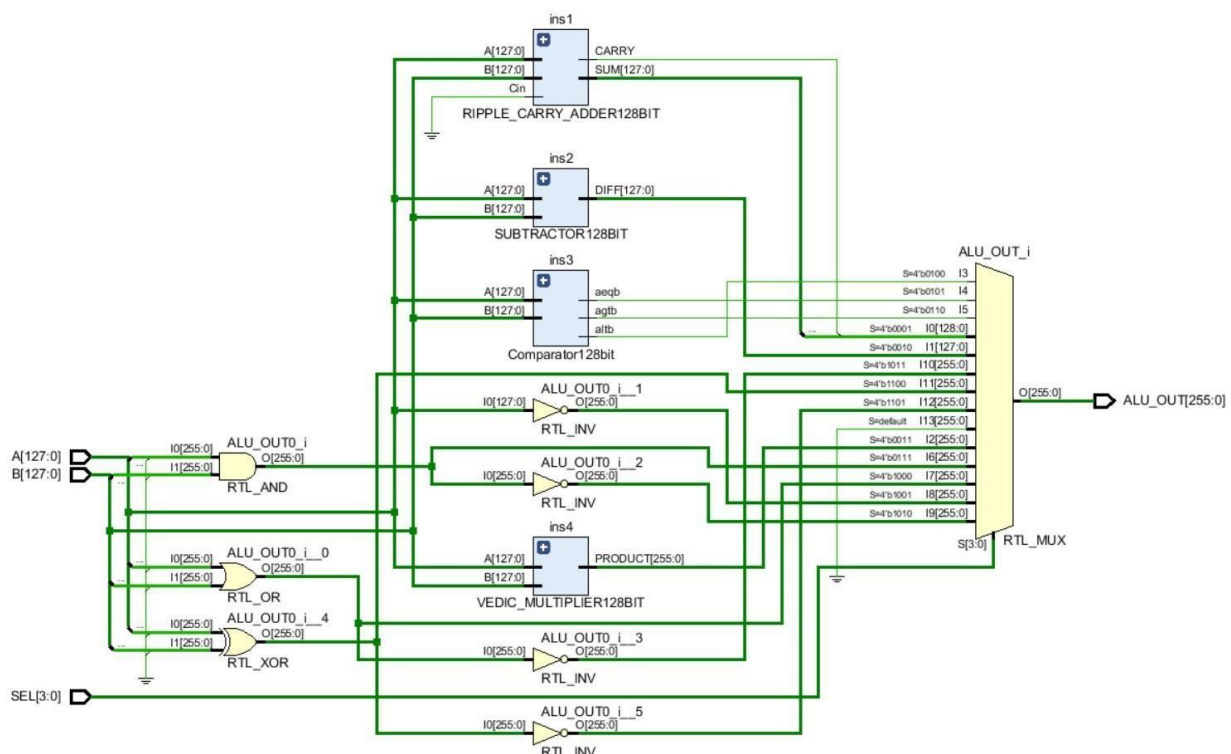


Figure: 3 RTL Schematic

Circuit simulation involves utilizing software algorithms to create and analyze electronic circuit models, predicting and validating their performance and behavior. This process is crucial for mitigating the expense and time associated with fabricating electronic circuits, notably integrated circuits (ICs). By employing a circuit simulator, engineers can efficiently assess a circuit's behavior and performance before physical realization. Fig. illustrates the output generated from such simulations, providing insights into the circuit's functionality and allowing for optimizations or corrections to be made prior to production, thus streamlining the development process and minimizing potential errors and costs.

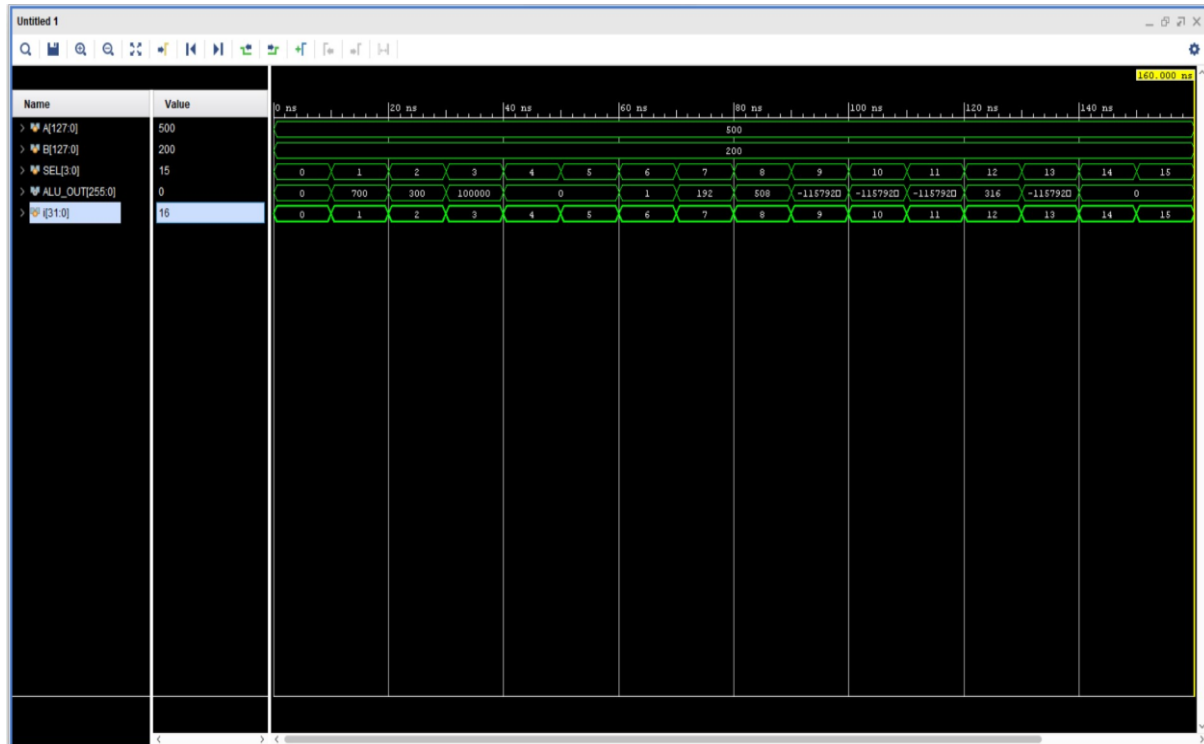


Figure:4 Simulation

6. CONCLUSION

Research has shown the efficacy of Vedic Mathematics principles over traditional methods across various mathematical tasks. In signal processing, computational units based on these principles have been proposed by numerous researchers, proving effective. The utilization of the Urdhva-Tiryakbyham Sutra in the proposed Vedic Mathematics-based Arithmetic Logic Unit (ALU) facilitates addition, logical operations, and multiplication.

The suggested ALU architecture finds applications in diverse signal processing tasks. Future integration of these structures promises to upgrade outdated integrated circuits, reducing the necessity for physical circuit board modifications.

This advancement not only enhances productivity but also ensures operational requirements are met. By leveraging Vedic Mathematics principles in circuit design, engineers can potentially streamline signal processing applications, leading to more efficient and cost-effective solutions in various technological domains.

7. FUTURESCOPE

The introduction of a 128-bit ALU utilizing Vedic mathematics presents intriguing avenues for future research and development. Exploring additional Vedic Sutras can expand the ALU's capabilities to encompass operations like division, square root extraction, and complex number arithmetic. Investigating pipelining techniques could enhance efficiency by enabling parallel processing of ALU sub-operations.

Integration with processor designs could optimize arithmetic-intensive algorithms across various computer disciplines such as signal processing, cryptography, and computer science. Co-designing hardware and software by integrating the Vedic ALU with software libraries tailored for Vedic algorithms can offer a holistic approach to performance optimization in computer systems. Moreover, exploring different hardware platforms beyond FPGAs, such as ASICs, could potentially improve performance and energy efficiency.

These paths signify promising directions for advancing computational efficiency and versatility in diverse technological domains.

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