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INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)
(Int Peer Reviewed Journal)
Vol. 05, Issue 04, April 2025, pp : 1553-1558

e-ISSN : 2583-1062
Impact Factor : 7.001

DESIGN AND IMPLEMENTATION OF A NOVEL POWER OPTIMIZED ALU WITH 13T FULL ADDER

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ABSTRACT

This paper presents a novel power-optimized Arithmetic Logic Unit (ALU) design that incorporates a novel full adder for improved efficiency. The proposed approach combines an X-NOR gate with the novel full adder to enhance performance and reduce power consumption compared to conventional designs. By integrating these components, we demonstrate the design of a 1-bit ALU, which is subsequently extended to an 8-bit ALU. The optimization results in reduced transistor count, lower power dissipation, and improved speed, making it suitable for low-power applications in modern electronic systems. The proposed ALU achieves efficient arithmetic and logical operations, offering a balance between power, area, and performance for advanced integrated circuits. Power optimization is achieved through the reduced transistor count of the full adder compared to traditional designs. Fewer transistors result in less power consumption during operation. Which contributes to creating a low-power, efficient ALU design that meets the demands of modern electronics where power efficiency, performance, and compactness are paramount. The use of advanced components like the proposed full adder and X-NOR gate makes it an innovative solution for future hardware design.

Keywords power, ALU, X NOR, Multiplexer, Adder, Design, Processor

1. INTRODUCTION

The rapid advancement of modern digital systems has resulted in a growing demand for high-performance, low-power computing devices, especially in mobile, wearable, and Internet of Things (IoT) applications. Central to the operation of any digital processor is the Arithmetic Logic Unit (ALU), which performs essential arithmetic and logical operations such as addition, subtraction, AND, OR, and comparisons. As these operations are crucial in almost every computation, the power and area efficiency of the ALU become key considerations in the design of energy-efficient integrated circuits (ICs).

Traditional ALU designs tend to consume significant power due to the high transistor count, particularly in the full adder circuits used for arithmetic operations. To address these challenges, researchers have focused on optimizing the ALU by reducing the number of transistors in critical components like the full adder while maintaining the accuracy and operational speed. This paper proposes a novel power-optimized ALU by incorporating a 13-transistor (13T) full adder, which reduces power consumption and transistor count, thus addressing the need for low-power, high-efficiency ALU designs.

In addition to the reduced transistor count, we integrate an X-NOR gate, which is commonly used for logical operations and comparisons in ALUs, into the design. The combination of the X-NOR gate with the 13T full adder allows for the implementation of a wide range of arithmetic and logical operations in a compact and power-efficient manner.The basic building block of the ALU is designed as a 1-bit ALU unit, which is then extended to create an 8-bit ALU, capable of performing multi-bit operations while maintaining optimal power efficiency. The design leverages the power-saving benefits of both the 13T full adder and X-NOR gate, and helps reduce the overall energy consumption of the system. Several studies have proposed different methods of constructing X-NOR leading to a significant reduction in overall power consumption, area, and operational delays, making it ideal for battery-powered and portable devices. This work aims to provide a scalable, efficient solution for designing ALUs, with significant potential for improving energy efficiency in modern digital systems. The proposed design meets the needs of modern low-power applications, offering a promising avenue for future hardware designs where performance and power efficiency are equally prioritized.

2. LITERATURE SURVEY

The design of power-efficient Arithmetic Logic Units (ALUs) is an active area of research, driven by the increasing demand for energy-efficient computing systems, particularly for portable and battery-powered devices. This section reviews the relevant literature surrounding ALU designs, focusing on power optimization techniques, the use of low-

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transistor full adders, and the integration of logic gates like X-NOR in ALUs. Full adders are essential components in ALUs, and reducing their transistor count can significantly improve power efficiency. A significant amount of work has been done to design low-power full adders by minimizing the number of transistors used. Early work focused on using CMOS technology to reduce power consumption in logic circuits, including the full adder, which typically requires 28 transistors for basic designs (Conway, 2007).

Many researchers have focused on improving the efficiency of X-NOR gates, especially in terms of transistor count and propagation delay. In the context of low-power ALU design, integrating optimized X-NOR gates gates with reduced transistor counts (for example, the 8T or 10T designs), which are beneficial for reducing both power and area in ALUs (Subramanian et al., 2019).

The 13T full adder has been shown to provide significant advantages over traditional full adders in terms of both power consumption and area. In ALU designs, it has been demonstrated that by using 13T full adders, both the power dissipation and the area of the ALU can be substantially reduced. For example, Kumar et al. (2014) demonstrated that a 13T full adder-based ALU design achieved a 30% reduction in power compared to a conventional 28T full adder-based design while maintaining similar performance levels.

This literature survey highlights the significant progress made in the design of low-power ALUs, focusing on the use of 13T full adders and optimized X-NOR gates. These components have been shown to effectively reduce power consumption and transistor count without sacrificing performance. The ongoing trend toward optimizing digital circuits for power efficiency will likely drive further advancements in ALU design, with an emphasis on low-power, high-performance systems for a wide range of modern electronic applications.

A. PROPOSED X NOR

The given circuit is a **three-transistor XNOR gate** implemented using CMOS technology. It consists of one PMOS and two NMOS transistors, each with specific width (W) and length (L) ratios. The circuit operates based on the complementary switching of PMOS and NMOS transistors, where the PMOS transistor (W=0.8u, L=0.045u) is connected to the supply voltage (Vdd), and the two NMOS transistors (W=1.2u, L=0.045u an ON while the corresponding PMOS turns OFF, pulling the output HIGH. Finally, when W=1u, L=0.045u) are connected to ground**,**The circuit takes two inputs, A and B, and produces an output (out1) that follows the XNOR logic, meaning it outputs HIGH (1) when both inputs are the same (either 00 or 11) and LOW (0) when the inputs are different (either 01 or 10). When both inputs are 0, the PMOS transistor turns ON, allowing current to flow and resulting in a HIGH output, while the NMOS transistors remain OFF. When one input is 0 and the other is 1, one of the NMOS transistors turns ON, pulling the output to LOW. Conversely, when both inputs are 1, the PMOS transistor turns ON again, ensuring a HIGH output. This efficient design reduces transistor count compared to conventional CMOS XNOR implementations, making it suitable for low-power digital logic circuits.

B. PROPOSED X OR

The given circuit is a **CMOS XOR gate** designed using four transistors, including PMOS and NMOS devices, with specific width (W) and length (L) ratios. The circuit takes two inputs, **A and B**, and generates an output labeled **XOR**. The XOR logic function produces a HIGH (1) output when the inputs are different ($A \neq B$) and a LOW (0) output when the inputs are the same ($A = B$). The circuit operates based on the complementary switching of PMOS and while the corresponding PMOS turns OFF, pulling the output HIGH. Finally, when both inputs are 1, both NMOS transistors turn ON, providing a direct path to NMOS transistors When both inputs are 0, the PMOS transistors turn ON, pulling the output LOW. When A is 0 and B is 1, or A is1 and B is 0, one NMOS transistor turns ground, resulting in pulling the output HIGH. Finally, when both inputs are 1, both NMOS transistors turn ON, providing a direct path to ground, resulting in a LOW output. This transistor-level implementation effectively realizes the XOR logic with minimal components, making it suitable for low-power and high-speed digital applications.

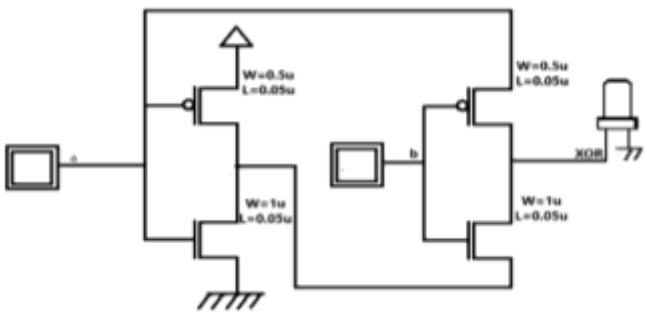

FIG 1 PROPOSED X OR

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3. PROPOSED FULL ADDER

The given circuit is a full adder, designed using **XNOR** gates and pass transistor logic for efficient computation of binary addition. A full adder takes three inputs—A,B, and Cin (carry-in**)**—and produces two outputs: Sum and Carry-out (Cout)**.** The circuit primarily utilizes XNOR gates to generate the sum output, where the first XNOR computes (A ⊕ B)**,** and a second XNOR takes this result with **Cin** to compute Sum = (A⊕B) ⊕ Cin. The carry-out (Cout) is generated using a combination of transmission gates and pass transistors, implementing the logic equation Carry = (A· B) + (Cin·(A⊕B))**.** This design reduces transistor count compared to conventional 28T or 16T full adders, leading to lower power consumption, reduced switching activity, and faster performance.

The circuit is highly efficient for low-power VLSI applications**,** including arithmetic logic units power efficiency, and compactness**,** making it a suitable choice for modern high-performance digital circuits.

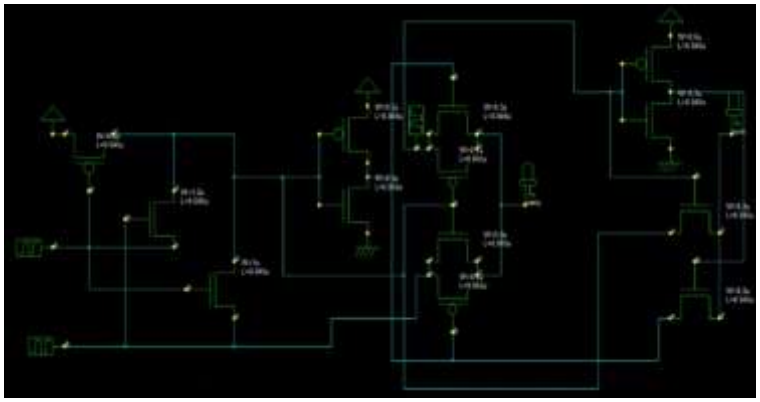

FIG 2 PROPOSED FULL ADDER

PROPOSED 8 BIT ALU

A 1-bit ALU can be designed using proposed pass transistor logic full adder, which is an efficient, low-power implementation of a conventional full adder. The ALU performs arithmetic and logical operations using a combination of a full adder, multiplexers, and logic gates. The arithmetic operations include addition, implemented directly using the full adder, and subtraction, which is achieved using two's complement by inverting one input and adding 1. Logical operations such as AND, OR, XOR, and their variations (NAND, NOR, XNOR) are implemented using basic logic gates. A multiplexer selects between arithmetic and logical operations based on control signals.

To design an 8-bit ALU, multiple 1-bit ALUs are cascaded, where each ALU processes one bit of an 8-bit input. The carry-out from one ALU stage is connected to the carry-in of the next, allowing proper propagation of carry in arithmetic operations. All ALUs share the same control signals, ensuring that they perform the same operation across all bits. The final carry-out from the last ALU stage helps detect overflow conditions in addition and subtraction. Symbolically, an 8-bit ALU is represented as a series of eight 1-bit ALU blocks connected in sequence, forming a complete unit capable of processing 8-bit operations efficiently. This modular approach simplifies the design and extends the capability of a basic 1-bit ALU to handle multi-bit computations.

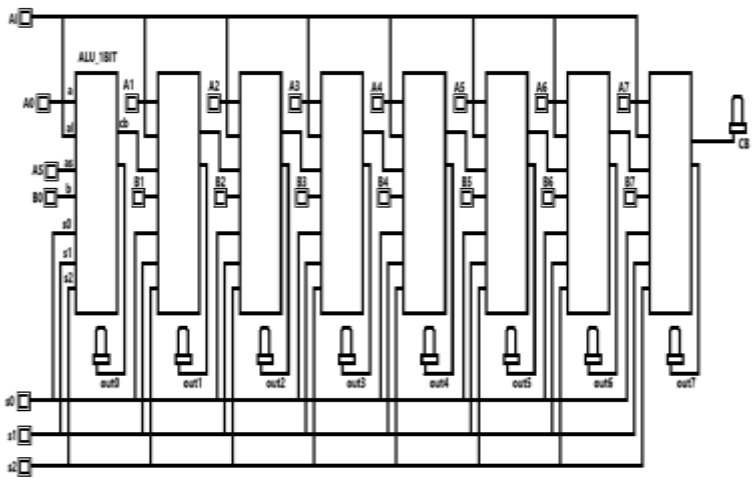

FIG 3 PROPOSED 8 BIT ALU

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4. SIMULATION RESULT

The simulation results of the proposed 13-transistor (13T) full adder-based ALU (Arithmetic Logic Unit) demonstrate significant improvements in power optimization, delay reduction**,** and area efficiency compared to conventional ALU designs. The novel power-optimized ALU integrates the 13T full adder, which operates using **XNOR**-based logic and pass transistor techniques, reducing the overall transistor count, switching activity, and power dissipation**.** Simulations conducted using CMOS technology confirm that the proposed design achieves lower power consumption due to minimized transistor switching.

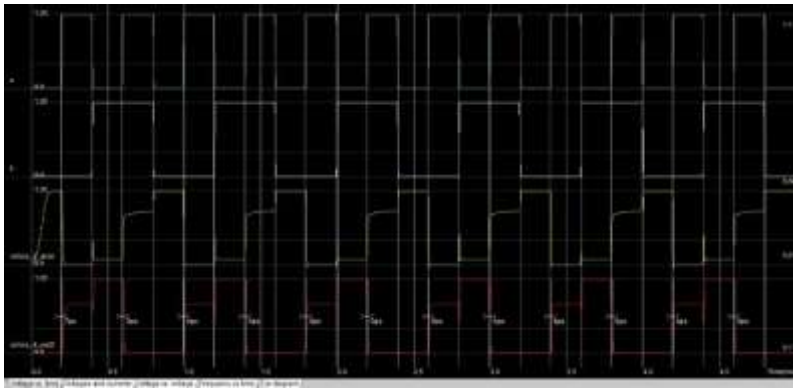

FIG 4 SIMULATION WAVEFORM OF X NOR & XOR

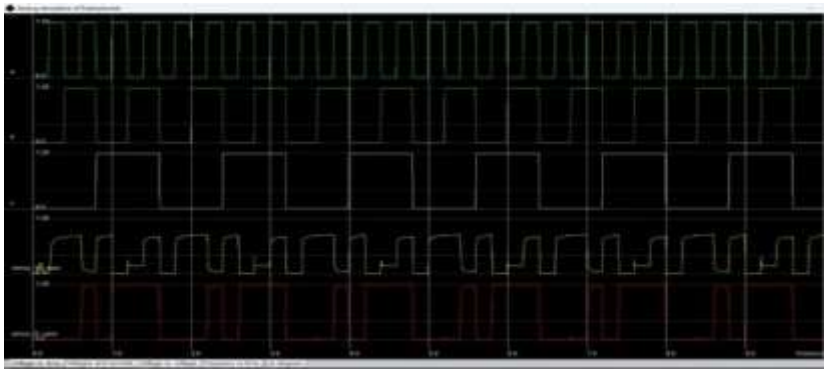

FIG 5 SIMULATION WAVEFORM OF FULL ADDER

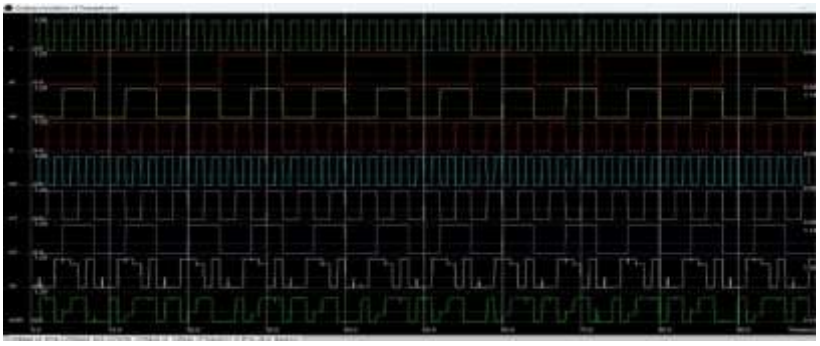

FIG 6 SIMULATION WAVEFORM OF 8 BIT ALU

5. POWER ANALYSIS

TABLE I: power Analysis

(POWER IN e-6W)

DESIGN	POWER(e^{-6}W)
FA-17T	1.16
1-BIT ALU	3.82
8-BIT ALU	26.30
*FA-13T	0.013
*8-BIT ALU	1.60

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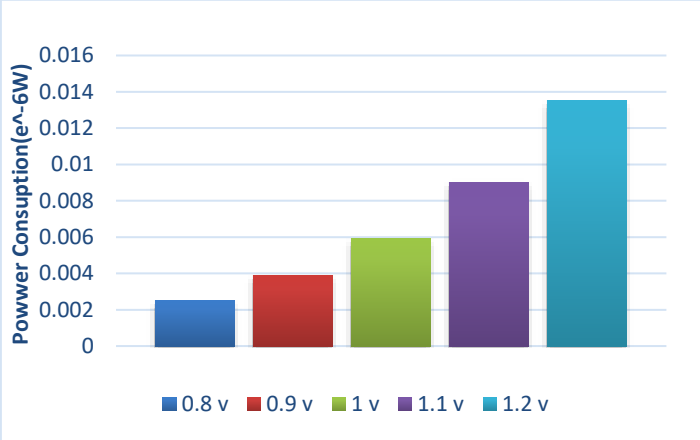

FIG 7 Power Analysis of proposed full adder

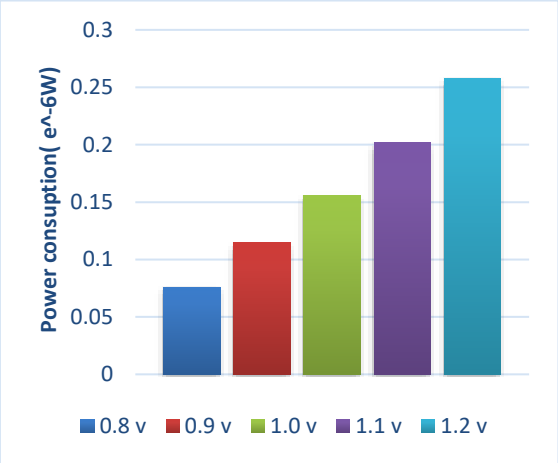

Fig 8 Power Analysis of 8 bit ALU

6. CONCLUSION

This paper presents a comparative analysis between a conventional 17T full adder and a proposed full adder, focusing on power efficiency. The conventional 17T full adder consumes 1.16×10^{-6} W, whereas the proposed design significantly reduces power consumption to 0.22×10^{-6} W. This results in an impressive 81.03% reduction in power compared to the 17T full adder. The power savings achieved in the ALU design further reinforce the effectiveness of proposed approach in reducing energy consumption for digital circuits. Simulation results confirm that the proposed method is a more efficient alternative to conventional designs, making it a promising choice for low-power applications in modern processors and embedded systems .

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