www.ijprems.com
editor@ijprems.com

INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)
(Int Peer Reviewed Journal)
Vol. 05, Issue 03, March 2025, pp : 459-463

e-ISSN : 2583-1062
Impact Factor : 7.001

DESIGN AND ANALYSIS OF 2:1 MUX USING DIFFERENT LOGIC FAMILIES FOR LOW POWER CONSUMPTION

R. P. Meenaakshi Sundhari[1], R. Bharathkumar[2], G. Maadesh Kannan[3], M. Jeganath[4],

[1]Professor, Department of ECE, P. A. College of Engineering and Technology, Pollachi, Coimbatore, India.

[2,3,4]UG Scholars, Department of ECE P. A. College of Engineering and Technology, Pollachi, Coimbatore, India.

Email.: rpmeenaakshi@gmail.com

DOI: https://www.doi.org/10.58257/IJPREMS38838

ABSTRACT

This paper compares 2:1 mux with various logic approaches (transmission gate, pass-transistor, and CMOS logic). As a consequence, it has been determined that a 2:1 mux built using TGL consumes the least power. It consumes lower power than pass- transistor logic, but PTL consumes high power than CMOS. Because the PTL mux uses the fewest number of transistors, it is the most space-effective circuit for constructing 2:1 MUX, but its performance is best in TGL as compared to other logics.

Keyword: Power consumption, Pass-transistor, Transmission Gate.

1. INTRODUCTION

Modern technology relies heavily on Very Large Scale Integration (VLSI), which allows the creation of integrated circuits (ICs) by densely packing billions of transistors onto a single chip. This advanced technology reduces the physical space required for semiconductors, minimizes delays in processing, and lowers power consumption in various electronic devices.

In communication networks, a multiplexer (mux) plays a crucial role. It converts serial data into parallel data, effectively combining multiple inputs onto a single data transmission line. This optimizes channel usage. The 2:1 MUX, for instance, has two inputs, one output, and a select line. The select line's binary value determines which input is routed to the output. This article explores the design of a 2:1 MUX using transmission gate, pass-transistor, and Complementary Metal-Oxide-Semiconductor logic. It also analyses the number of transistors required for these designs and their respective power consumption. A multiplexer is a versatile circuit that may be used to build many logic gates. The mux is a digital switch with 2n input lines, 'n' select lines and one output line. Output is generated by connecting to the selected data input line and executing the binary combination of the specified lines.

A 2:1 multiplexer (MUX) has two input data channels (X0 and X1), one selection channel (S), and one output channel (Y). Based on the binary value of the selection channel, the MUX switches between the two input channels. When S is "0", the data from input X0 is routed to the output Y. When S is "1", the data from input X1 is routed to the output Y. The Logical equation and structural diagram of 2:1 MUX are provided below:

$Y = X_0 \overline{S} + X_1 S$

Figure 1.2 depicts a 2:1 MUX logic circuit made up of fundamental logic gates such as AND, OR, and NOT.

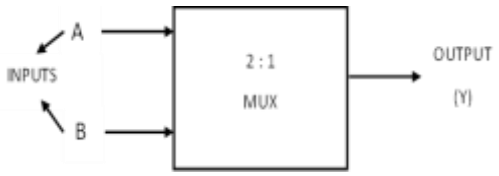

Figure 1.1: 2:1 MUX BLOCK DIAGRAM

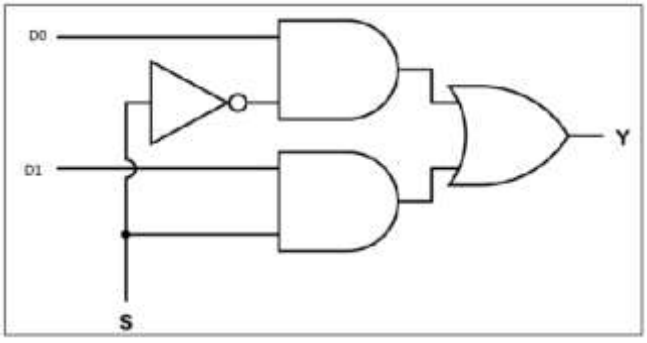

Figure 1. 2 : 2:1 MUX LOGIC DIAGRAM

www.ijprems.com
editor@ijprems.com

INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)
(Int Peer Reviewed Journal)
Vol. 05, Issue 03, March 2025, pp : 459-463

e-ISSN : 2583-1062
Impact Factor : 7.001

The truth table displays all input combinations of the selection line and data inputs. When the selection line is low (0), the output matches the data input X0, regardless of the other data inputs. Conversely, when the selection line is high (1), the output becomes identical to data input X1, irrespective of X0's value.

Table 1 : 2.1 MUX Truth Table

X0	X1	S	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

1.1 MUX USING TRANSMISSION GATE

A transmission gate is like a switch made up of two transistors, one PMOS and one NMOS. These transistors control the flow of signals from the input to the output of the gate. To switch the signal, you use control signals applied to the gates of the transistors. When the control signal is "on," both transistors turn on and let the signal through. When the control signal is "off," both transistors turn off and block the signal. You can use transmission gate logic to build circuits that select between different data lines. For example, a 2:1 multiplexer using this logic has four transistors. When a logic "0" is applied to the control input, transistors N1 and P1 turn on like short circuits, allowing data from line A to pass through. At the same time, transistors N2 and P2 turn off like open circuits, blocking data from line B. Data A is sent to the output.

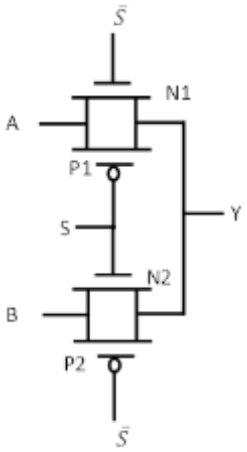

Figure 1.2, 2.1. MUX USING TRANSMISSION GATE

When 'S' equals '1', transistors N1 and P1 become inactive (open), while N2 and P2 become active (short circuits). This allows data from input B to flow directly to the output through a single conducting path.

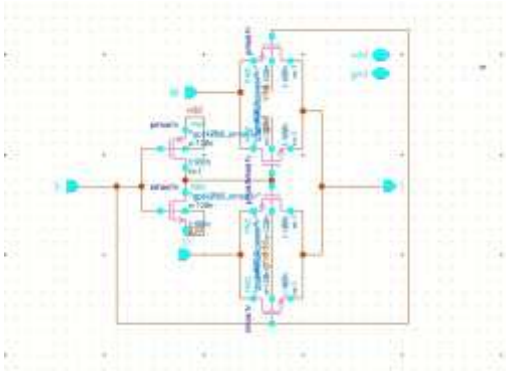

Figure 1.3 : CIRCUIT DIAGRAM FOR 2:1 USING TRANSMISSION GATE

www.ijprems.com
editor@ijprems.com
INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)
(Int Peer Reviewed Journal)
Vol. 05, Issue 03, March 2025, pp : 459-463
e-ISSN : 2583-1062
Impact Factor : 7.001

The circuit is simulated in 45nm technology using cadence tool with a 1V power supply to get the desired output. Waveforms acquired following simulation are depicted in Figure 2.3:

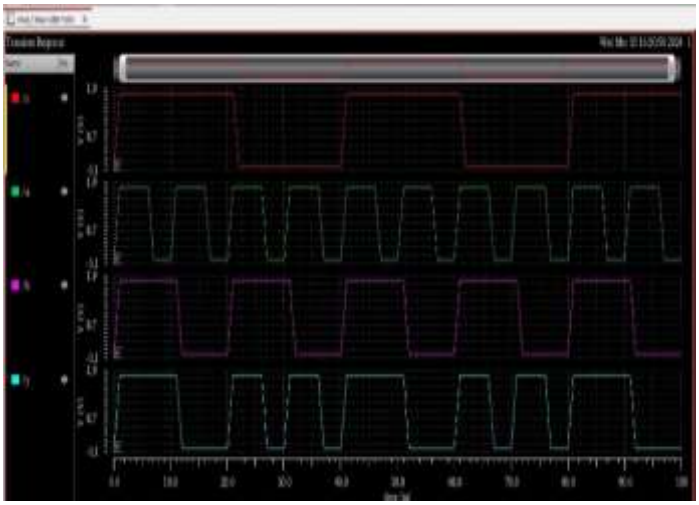

Figure 1. 4 : 2.1 Simulation waveform of 2:1 MUX using Transmission Gate

MUX USING PASS-TRANSISTOR LOGIC

As the name indicates, a pass-transistor operates on logic applied from outside as a control signal at the transistor's gate. It is used to reduce transistor count while increasing logic circuit performance by deleting superfluous transistors. A 2:1 multiplexer may be created using Pass-transistor logic with only two NMOS transistors. Figure 3.1 shows the circuit that was designed.

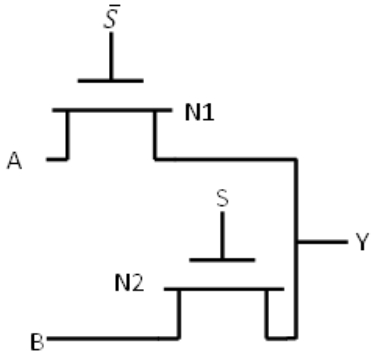

Figure1.5 : 2.1 PASS-TRANSISTOR LOGIC OF 2:1 MUX

Two data signals, A and B, are routed to the terminals of pass-transistors N1 and N2. When the control signal S is inactive (low), N1 activates, creating a direct path between input A and the output. Meanwhile, N2 is inactive, blocking input B. Conversely, when S is active (high), N1 deactivates, while N2 activates, establishing a direct path between input B and the output. As a result, the output mirrors input B. The circuit's operation is illustrated through input and output waveforms generated using a 1V power supply.

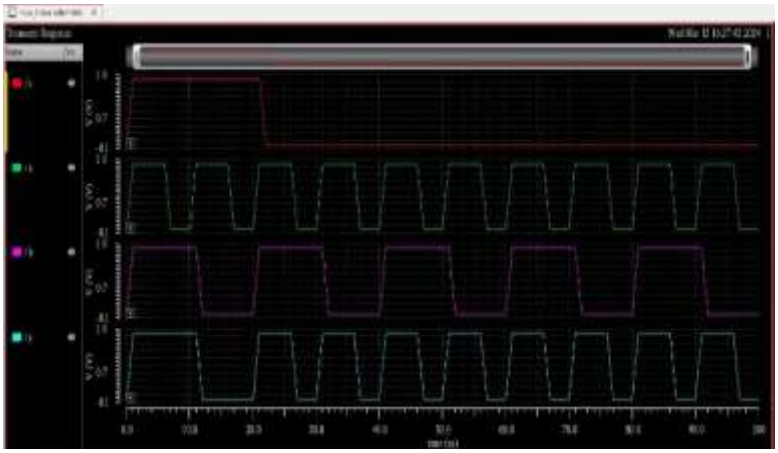

Figure 1.6 : 2.1 Output waveform of 2:1 MUX using Pass-transistor Logic

www.ijprems.com
editor@ijprems.com
INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)
(Int Peer Reviewed Journal)
Vol. 05, Issue 03, March 2025, pp : 459-463
e-ISSN : 2583-1062
Impact Factor : 7.001

COMPLEMENTARY METAL-OXIDE-SEMICONDUCTOR (CMOS) LOGIC BASED 2:1 MUX

CMOS logic, which employs a symmetric number of both PMOS and NMOS MOSFETs, improves circuit performance by providing complete '1' and '0' logics at the output without distortion. A 2:1 MUX in CMOS is simulated using ten transistors. Figure 8 depicts the circuit that was designed. There are equal number of PMOS and NMOS transistors.

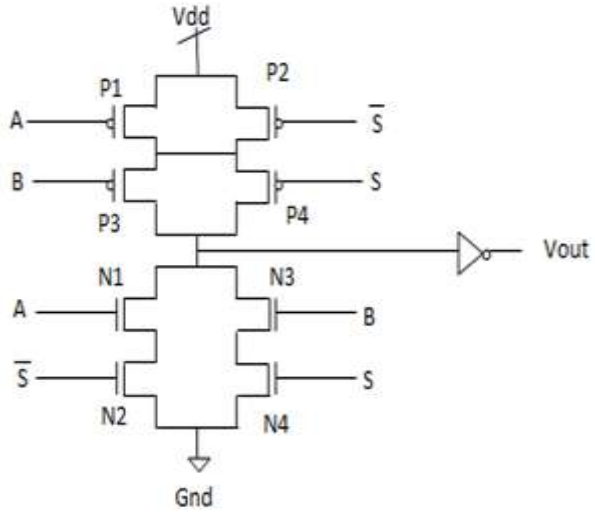

Figure 1.7 2.1 MUX USING TRANSMISSION GATE

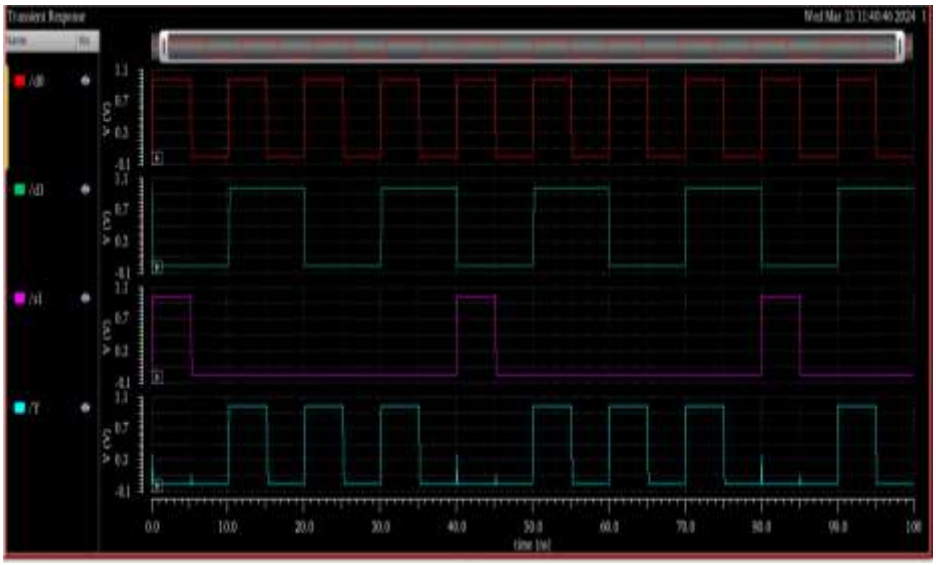

Figure 1.8 2.1 Output waveform of 2:1 MUX using Complementary Metal-Oxide-Semiconductor (CMOS) logic

Figure 4.2 shows waveforms for inputs and outputs produced from the simulation of the circuit in Cadence. Simulations of CMOS multiplexers are performed at 45nm technology.

2. COMPARATIVE ANALYSIS

The 2:1 Multiplexer (MUX) is created using Transmission Gate Logic (TGL), Pass-Transistor Logic (PTL), and Complementary Metal-Oxide-Semiconductor (CMOS) circuits. Simulations of all circuits were performed using 45nm technology, powered by a 1V supply, with power consumption recorded in every instance. Multiplexers developed using transmission gates and CMOS consume significantly less power than those designed with pass-transistor logic. When compared to the three circuits with different design methodologies, the 2:1 multiplexer built with TGL uses the least amount of electricity. While the power usage of Transmission Gate Logic and Complementary Metal-Oxide-Semiconductor (CMOS) circuits is similar, The number of transistors employed in their designs exhibits significant variation.

To achieve a 2:1 MUX, Complementary Metal-Oxide-Semiconductor (CMOS) requires three times as many transistors as the TGL approach. The PTL multiplexer is the most space-efficient logic circuit for 2:1 MUX since it contains the fewest transistors, namely two. However, its performance is low because the output is significantly distorted. When compared to TGL and PTL circuits, CMOS requires a high number of transistors but has excellent performance and a rapid switching time, thus the delay is low.

www.ijprems.com
editor@ijprems.com
INTERNATIONAL JOURNAL OF PROGRESSIVE RESEARCH IN ENGINEERING MANAGEMENT AND SCIENCE (IJPREMS)
(Int Peer Reviewed Journal)
Vol. 05, Issue 03, March 2025, pp : 459-463
e-ISSN : 2583-1062
Impact Factor : 7.001

The comparative analysis of the three logic is given in Table 2.

Table 2 : 2.1 Comparison Table

Circuit	Transistor count	Input Voltage	Power Consumption (watts)
Transmission Gate	4	1V	2.7451E-09
Pass-transistor	2	1V	1.1205E-06
CMOS	10	1V	7.0856E-09

3. CONCLUSION

This study investigates the power consumption of 2:1 mux implementation that employ Pass-Transistor Logic, Transmission Gate Logic, and Complementary Metal-Oxide-Semiconductor (CMOS) Logic. The circuit is simulated with the Cadence tool, 45nm technology, and a 1V power supply. TGL and CMOS logic-based 2:1 muxes need nanowatts of power, whereas PTL versions use microwatts. The 2:1 mux designed with TGL uses the less amount of power.

4. REFERENCES

[1] S. Abirami, M. Arul Kumar, E. Abinaya and J. Sowmaya, "Design and analysis of 2: 1 multiplexer circuit for high performance", International Journal of Electrical and Electronics Engineers Vol., no. 7, Jan-June 2015.

[2] K. Yano, Y. Sasaki, K. Rikino and K. Seki, "Top-down pass-transistor logic design", IEEE Journal of Solid-State Circuits, vol. 31, no. 6, pp. 792-803, 1996.

[3] Monika Mehra ,R P Singh – Multiplexer using various styles of design . Journal of Emerging Technologies and Innovative Research www.jetir.org September (2018).

[4] Ekansh Agarwaal, Divyanshu Maheshwari -Comparative Analysis of MUX Using Various CMOS Circuit Style under Nanometer Technology. International Journal of Creative Research Thoughts (IJCRT) www.ijcrt.org August (2021).

[5] Ila Gupta, Neha Arora, Prof. B. P. Singh / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 2, Mar-Apr 2012, pp.1492-1496.