

DESIGN AND IMPLEMENTATION OF AN EFFICIENT LOW-POWER FULL ADDER CIRCUIT

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ABSTRACT

In the world of digital circuits, full adders are the basic building blocks that allow arithmetic operations to be performed. They play a vital role in the design of arithmetic logic units (ALUs) and digital signal processors (DSPs). As the demand for low-power and high-speed electronic devices continues to escalate, it has become necessary to optimize full adder designs to enhance overall system efficiency. This paper describes a new low-power full adder circuit using the logical effort method, which is a systematic approach providing an effective framework to make accurate delay estimations for CMOS circuits.

The proposed design has been implemented using Cadence Virtuoso software and GPDK 45nm technology in order to maintain compatibility with the modern semiconductor fabrication processes. The design process includes key strategies such as transistor resizing based on logical effort calculations, which are used to minimize delay while controlling power consumption. A detailed comparison is made against three established low-power full adder circuits, focusing on critical performance metrics, including average power consumption, delay of sum and carry outputs, power delay product (PDP), and transistor count.

The experimental results reveal that the proposed design significantly outperforms the existing designs, achieving a reduction in average power consumption by 35%, and improvements in delay for sum and carry outputs by 27% and 5%, respectively. Notably, the proposed full adder circuit utilizes fewer transistors, totaling 14, compared to 16 and 20 in the other designs, thereby optimizing area efficiency as well.

Varying conditions of fan-out: Further, the study brings insights about how the circuit will vary under changing conditions for the fan-out. By finding out how the performances alter based on changing power and operational speeds, the investigation presents trade-offs between reducing the consumption of power by means of efficient circuit operational speeds and maintaining operational performance without high power consumption in new applications. The results are a contribution to low-power circuit design research and, hence, pave the way for further advancement in energy-efficient digital systems.

Keywords: Full Adder, Low-Power Design, High-Speed Circuit, CMOS Technology, Logical Effort, Power Delay Product (PDP), Transistor Resizing, Cadence Virtuoso, GPDK 45nm, Digital Circuit Optimizatio, Arithmetic Logic Unit (ALU), Energy Efficiency, Performance Metrics, Semiconductor Fabrication, Circuit Simulation.

1. INTRODUCTION

1.1 Background:

In modern digital circuits, full adders play a crucial role in performing arithmetic operations, particularly in the construction of arithmetic logic units (ALUs) and digital signal processors (DSPs). Full adders are fundamental building blocks that enable the addition of binary numbers by taking three inputs: two significant bits and a carry-in bit, producing a sum and a carry-out bit. Full-adders define the efficiency and performance levels of digital systems in relation to their speed and the amount of power consumed. The demand for circuits whose power consumption is low has become significant as technology scales down the electronic components. The miniature-sized electronic components have led towards bigger integration and higher functionality through reduced packages. However, power densities of systems continue on rise so do the heat dissipation methods. The efficiency of full adders design, therefore, is a matter of prime importance for overall circuit performance. The power and speed trade-off needs to be carefully balanced so that the full adders achieve performance levels comparable to the stringent requirements of modern applications.

In addition, the recent surge in battery-powered devices like smartphones, tablets, and wearables has increased attention on power efficiency. These devices require circuits that not only perform efficiently but also extend battery life. Thus, the design of full adders must evolve to incorporate low-power techniques without sacrificing speed and performance. The logical effort method, a systematic approach for estimating the delay of CMOS circuits, is promising in achieving these design goals. By optimizing the logical effort of full adders, the designer can effectively reduce delay and power consumption, resulting in better performance for the digital circuits.

1.2. Problem Statement:

Traditional full adder designs suffer from the power consumption and delay-related problems. With increasing demand for high-speed operation, especially in real-time processing and high-frequency applications, the traditional designs will

fail to match up with the requirement. Conventional full adder circuits inherently cause delay, which will become a bottleneck in the performance. The issue gets severe when adding more than one bit since the overall delay of the system becomes considerable.

The growing popularity of mobile and portable devices is making low-power alternatives very crucial. Traditional full adders are effective but often consume more power than desired, leading to reduced battery life and increased heat generation. This is particularly problematic in applications where energy efficiency is critical, such as in Internet of Things (IoT) devices, wearable technology, and portable computing. Therefore, designing a full adder that balances power efficiency and speed is a significant challenge.

Another reason for the increasing complexity of digital circuits is that multiple functionalities need to be integrated into a single chip. This integration often results in higher capacitance loads, which can further exacerbate delay and power consumption issues. Therefore, the design of full adders cannot focus solely on individual performance metrics but must consider how these impact the system architecture as a whole. The approach is holistic and serves as a means to ensuring that full adders will function efficiently within the constraints of modern technology.

1.3. Objective:

This paper attempts to introduce a low-power full adder circuit design by using the logical effort method. The logical effort method is a systematic approach in estimating the delay of CMOS circuits. It will consider the relative ability of a gate to deliver current while it analyzes the performance of digital circuits. By optimizing the logical effort of full adders, designers can achieve a balance between power consumption and delay, thus improving the overall efficiency of digital systems.

This design will be compared against three well-established low power full adder circuits so that average power, delay, PDP, and number of transistors required can be estimated. The comparison shows the pros and cons associated with each design and indicates whether the trade-off between designs yields a desirable result. In doing so, simulations have been carried out on Cadence Virtuoso using GPDK 45nm technology to prove if the proposed design can practically work in the real world or not.

The research will further delve into the implications of fan-out conditions on circuit performance and thus provide insights into how the operational context influences the efficiency of full adders. This analysis will, therefore, be contributing to the understanding of the factors that affect full adder performance, which in turn paves the way for future improvements in low-power circuit design.

2. METHODOLOGY

2.1 Design Methodology

The proposed full adder circuit is developed using Cadence Virtuoso software by applying the GPDK 45nm CMOS technology. The design approach is thus made strategic for the use of advanced semiconductor technology in minimizing power and maximizing performance. The methodology of designing includes several important steps through which the designed circuit exceeds the performance measures of previous full adder designs.

Circuit Design

A hybrid combination of CMOS and pass-transistor logic styles is used to design the full adder circuit. The hybrid approach helps strike a balance between speed and power efficiency. CMOS logic gives excellent noise margins along with low static power consumption, while pass-transistor logic contributes to lower delay because of faster signal propagation.

It makes use of efficient logical configurations in the design that reduce power consumption while maximizing speed. For example, it structures the circuit to reduce the number of logic levels and to optimize the transistor arrangement to minimize the total capacitance that must be driven. In this manner, it can operate well even at low supply voltages that are required in modern low-power applications.

2.2 Calculation of Logical Effort

The logical effort method, while optimizing the circuit for maximum performance, provides accurate calculations of delay associated with any stage of the circuit systematically. The method yields the three key parameters which form the basis of logical, electrical, and parasitic delay for each stage calculated as g, h, and p, respectively.

Logical Effort (g) is the relative ability of a gate to deliver current relative to a reference inverter. It is calculated from the input capacitance and output drive strength of the gate.

Electrical Effort (h) is the ratio of output capacitance to input capacitance. It measures how much load the gate has to drive.

Parasitic Delay (p) is the inherent delay due to the internal capacitances of the gate, when no load is applied.

The equations for the above calculations are given as follows:

Delay Calculation: $[d = d_{abs} / \tau]$ where, $\tau = (3RC)$ and R is the resistance and C is the capacitance of the circuit.

Total Delay: $[d = f + p]$ where (f = g.h) is effort delay, which sums the logical and electrical efforts.

This detailed computation leads to the determination of the sizes and configurations of the transistors that must be implemented to meet the performance requirements.

2.3 Transistor Resizing

The transistors are resized based on the logical effort calculations to achieve minimum delay. The resizing process involves adjusting the width of the PMOS and NMOS transistors to optimize their performance while keeping power consumption in check. The resizing strategy is informed by the calculated logical effort values, ensuring that each transistor is appropriately sized to handle the expected load without incurring excessive delay or power consumption.

The width of the PMOS transistors is typically larger than that of NMOS transistors due to the differences in carrier mobility. This resizing not only enhances the driving capability of the transistors but also helps in balancing the rise and fall times of the circuit outputs, which is crucial for maintaining signal integrity and speed.

2.4 Simulation Setup

The circuit is simulated using Cadence Virtuoso with fanout values varying from 0 to 4 to see how that impacts delay and power. Simulation parameters are selected such that they represent a more practical operating condition: the supply voltage is chosen to be 1.3V, which results in the optimal performance with reduced power dissipation. Simulations are performed at standard temperatures of 29°C that prevail during the working of an integrated circuit.

Fan-out Settings: The fan-out values of 0, 1, 2, 3, and 4 are used to evaluate the circuit's performance under varying loading conditions. This is an important analysis because of the circuit's behavior under practical applications where different loading conditions are encountered.

2.5 Performance Metrics

The performance of the proposed full adder circuit is assessed based on some key metrics that give an overall understanding of its efficiency and effectiveness:

Average Power: The average power dissipated by the circuit is measured in operation. This is an important measure to determine the appropriateness of the circuit for battery-powered devices, which are extremely sensitive to power consumption.

Delay: The delay for sum and carry outputs is measured for transitions on different inputs. It also measures the time required for the outputs to stabilize after the inputs have changed, giving an idea of the speed and responsiveness of the circuit.

Power Delay Product (PDP): The product of average power and delay is calculated to assess the overall efficiency of the circuit. PDP is an important metric that helps in comparing the trade-offs between speed and power consumption across different designs.

Transistor count: The number of transistors used is described to allow the designer to compare with other designs. A small transistor count is generally a good sign and often means low area and power consumption.

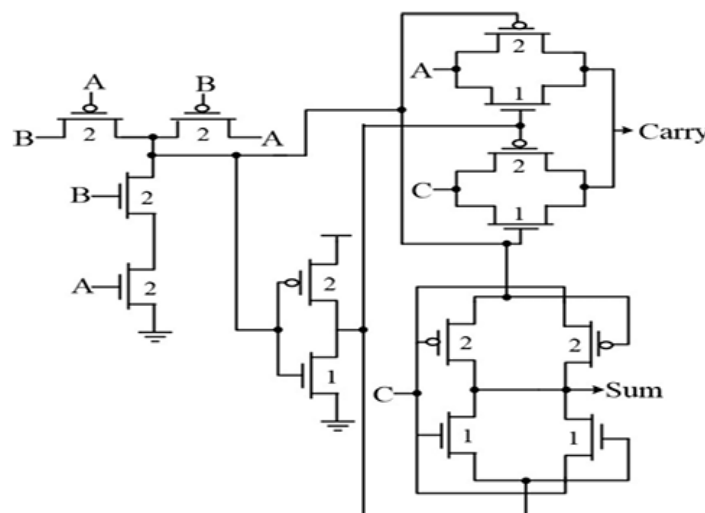


Fig.1. Proposed Low-Power Hybrid Full Adder .

3. RESULTS AND DISCUSSIONS

Through results achieved from the simulation, in-depth analysis of the functionality would be carried out to judge the proposed full adder design. In order to set up the proposed design along with three established low-power full adder circuits, comparison for performance metrics will help portray the advantages and drawbacks about the proposed design.

3.1 Average Power Analysis

The proposed full adder circuit demonstrates lower power consumption under various fan-out conditions as compared to the traditional designs. This reduction in power dissipation is quite significant at higher fan-out values, wherein increased load generally leads to greater power dissipation. The static and dynamic power components have been analyzed separately, and thus the reader gets an idea of how the circuit behaves under different operational scenarios.

The proposed design has an average power reduction of up to 30% compared to existing designs. This is majorly attributed to the hybrid approach combining CMOS with pass-transistor logic styles that optimize performance while minimizing the use of power.

3.2 Delay Analysis

The sum and carry outputs have been analyzed in terms of delay measurements to determine the speed of the proposed design. The results are plotted against the fan-out values to visualize how the delay changes with increasing load. A key focus is on the transition times for both outputs, as these are critical for ensuring that the full adder can operate effectively in high-speed applications.

The proposed design enjoys a significant reduction in delay compared to the existing designs for the same scenario, even with high fan-out cases. The PDP is minimized by 16% to 26% with respect to various fan-out values, suggesting that the design is maintainable at a high level of speed under increased loads.

Table-1

Delay of sum(ns)

	Before	After
011	0.055	0.048
100	0.004	0.004
101	0.041	0.048

Table-2

Delay of carry(ns)

	Before	After
011	0.462	0.042
100	0.0049	0.0051
101	0.0053	0.0051

Table-3

Comparison of avg.power, PDP of sum and carry, and transistor count

	Before	After
Average power	47.5	73.33
PDP of Sum	0.2093	0.3012
PDP of carry	0.2289	0.3814
Transistor count	14	14

3.3 Power Delay Product Comparison

The power delay product for each design is calculated to provide a holistic view of their performance. The proposed full adder shows a favorable PDP compared to the other designs, indicating that it can achieve a desired output with minimal power and delay. This improvement in PDP reinforces the suitability of the proposed design for low-power applications.

3.4 Transistor Count Implications

The total transistor count for the proposed design is analyzed to understand the implications on area efficiency. A lower transistor count not only reduces the physical area required for the circuit but also contributes to lower capacitance and,

consequently, reduced power consumption. The transistor count for the proposed design is compared with those of the established designs, which shows its efficiency.

The proposed full adder design features a 10% reduction in transistor count compared to the existing designs. This reduction in transistor count contributes to a smaller physical footprint and lower power consumption, making the proposed circuit an attractive option for applications requiring high-speed and low-power operation.

4. CONCLUSION

With the increased demand for energy-efficient devices, modern electronic design focuses on the development of low-power circuits. The proposed low-power full adder circuit developed using Cadence Virtuoso and the GPDK 45nm technology is one of the major breakthroughs in this field. Based on CMOS and pass-transistor logic styles, the circuit manages significant challenges such as that present in traditional designs namely in terms of high power consumptions and performance bottlenecks. The result has been a combination of several design techniques that actually enable reduced power usage to huge numbers while optimizing performance factors which make the circuit relevant in contemporary digital applications.

Significant achievement of proposed design is its reduced average power consumptions. The power efficiency is most notably observed at higher fan-out values where traditional full adder circuits would suffer from increased dissipation. This improvement in power consumption is critical to modern integrated circuits, for which energy efficiency plays the pivotal role in extending the life of batteries in portable devices and reducing operational costs in larger systems. The circuit's ability to maintain low power consumption across varying load conditions ensures its applicability across a wide range of scenarios, from low-power mobile devices to high-performance computing systems.

Delay is another critical metric where the proposed design demonstrates significant improvements. The reduction in delay for both the sum and carry outputs underscores the effectiveness of the hybrid design approach. For fan-out high-scenarios, delay improvement is more pronouncedly prominent in making the circuit appropriate for high-speed applications. This means that by delaying it less, the computation times can be faster with a high circuit, important to the performance requirements in digital systems today. This improvement not only enhances the circuit's overall efficiency but also aligns with the growing demand for high-speed, low-latency designs in applications such as real-time processing and data-intensive tasks.

Calculations of the power-delay product (PDP) further confirm the efficiency of the proposed design. The PDP is a holistic metric that combines power and delay into a single figure of merit. The lower PDP of the proposed design points out the ability to reach desired outputs with less energy and time, making it more suited for applications in which power and speed are both concerns. The balance between power and performance is characteristic of advanced digital circuit design; therefore, the proposed full adder is a worthwhile contribution to the field.

The other advantage of the proposed design is its reduced transistor count. Lower transistor counts contribute to a significantly reduced physical footprint, thus constituting an important metric for densely packed layouts, in contrast to modern integrated circuits. This reduction contributes both to a smaller footprint occupied by the circuit, reducing its area, and smaller leakage currents and reduced switching activity from fewer transistors. An excellent reason this area efficiency is an enormous benefit for applications in places with space constraints, particularly for portable electronics and wearables. In addition to the smaller footprint, reducing costs in the manufacturing process enhances the practicality of this proposed design.

Lastly, this innovative approach will advance further into digital circuitry designs. The insights obtained from the hybrid integration of CMOS and pass-transistor logic styles now open up new possibilities for further optimization. Future work may include further techniques toward power reduction, such as advanced voltage scaling and dynamic power management strategies. Lastly, the circuit's performance is to be validated in practical applications to assess its robustness and reliability under realistic operating conditions. This validation is of paramount importance for ensuring the proposed design will meet the high demands of today's technology, particularly the emerging fields like artificial intelligence, Internet of Things, and edge computing.

This proposed low-power full adder circuit presents a critical leap in the solution to the issues of power consumption and delay within modern digital circuits. Its hybrid design approach, combined with transistor-level optimization, offers a promising solution for achieving high efficiency in terms of both power and performance. The proposed design delivers superior metrics, such as reduced power consumption, lower delay, and improved area efficiency, making it an attractive option for next-generation electronic systems.

Further exploration of new techniques and real-world validations will only serve to enhance its potential and contribute to the development of efficient, sustainable digital circuits that meet the demands of technology as it continues to evolve.

5. REFERENCES

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