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DESIGN OF 8-BIT APPROXIMATE MULTIPLIER USING SINGLE EXACT SINGLE APPROXIMATE ADDERS AND SINGLE EXACT DUAL APPROXIMATE ADDERS

Rangoori Sravani Sai[1], Ananda Kumari[2]

[1]P.G Scholor, Sanketika Vidya Parishad Engineering College, Visakhapatnam, India.

[2]Assistant Professor, Sanketika Vidya Parishad Engineering College, Visakhapatnam, India.

sravanisairangoori@gmail.com, anandaniigatti18@gmail.com

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ABSTRACT

An adder is the basic computational circuit in digital Very Large Scale Integration design. Approximate Adders have been proposed to improve the design metrics of an adder. Digital Multiplier is a fundamental component in many digital signal processing (DSP) systems, which takes up the most part of the computational resources. As many DSP applications have an inherent tolerance for inexact computations, approximate multiplication is considered as an appropriate substitution to obtain energy-performance-accuracy tradeoffs, especially in those applications that require high energy-efficiency in computing. Meanwhile, reducing the supply voltage is proved to be an efficient way to further lower the total energy consumption. In this paper multiplexer based approximate full adder is proposed for 8-Bit approximate multiplier and its circuit implementation is proposed for error-resilient multiplication with a low supply voltage. Simulation results indicate that the approximate multiplier with our proposed 8-Bit approximate multiplier consumes the least energy per operation with the same computational accuracy when compared with other multipliers for the operand length of 8 bits. It achieves 26.7% reduction on energy-delay product (EDP) when compared with the exact multiplication.

Keywords- Single Exact Single Approximate Adder, Single Exact Dual Approximate Adder, Approximate Multiplier, Power consumption, propagation delay.

1. INTRODUCTION

Computing efficiency of the adder with new circuit designs provides high performance and better result [2]. One of the recent [1] and efficient method is approximate computing. It is being used in many applications like computer vision, data mining, deep learning neural networks, video/image processing etc [3,4]. Approximate computing gives results which are less accurate but with acceptable quality by providing the stringent error requirement. Digital multipliers are always fundamental arithmetic units with important influence on performance of the entire system. A fast multiplier is typically composed of three parts: partial products generation, partial products compression, and a fast carry propagation adder (CPA) for the result. Among these three parts, the compression tree occupies the largest proportion in terms of area, delay and power consumption. Thus, energy efficient compressors are required in the multiplier design Intuitively, the partial products in a compression tree are accumulated with two operand adders, which use full adders, sometimes known as 3-2 compressors. Compared with full adders, 8-Bit approximate multiplier have a higher compression efficiency so that are widely used in a partial products reduction tree. In approximate multiplier design, many approximate 8-Bit approximate multiplier have been proposed to achieve high energy efficiency [3]-[6]. An approximation method is proposed in [3], which cuts the carry chains between two 8-Bit approximate multiplier of the same stage. It reduces the hardware complexity greatly but incurs a high error rate, and thus, a poor computational accuracy. In this paper, a multiplexer approximate adder based approximate 4-2 compressor is proposed with a complementary error strategy in order to obtain a reduced logic complexity with acceptable computation accuracy. In addition, the circuits are designed at a low supply voltage to achieve even higher energy efficiency.

2. EXISTING TECHNIQUES

2.1 SESA1 ADDER

In SESA1 adder, we introduce approximation in the SUM output by making it to be equal to the complement of CARRY. As seen from Table, SESA1 adder has errors in SUM bits for input combinations 000 and 111. The CARRY output remains same irrespective of whether SESA1 adder operates in exact or approximate mode. In exact mode, the SUM output is computed using a power gated (PG) controlled inverter whose input is the complement of SUM. In approximate mode, the SUM module is PG, and the approximate output which is made equal to the complement of CARRY is generated using another PG-controlled inverter whose input is connected to the complement of CARRY as shown in Figure.

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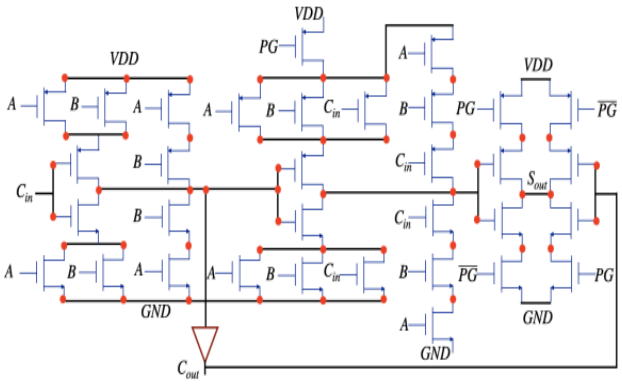

Figure 1: Circuit diagram of SESA1 adder

2.2 SESA2 ADDER

In SESA2 adder, we introduce approximation in the SUM output by making it 0 for all the input combinations as shown in Table for approximate mode.

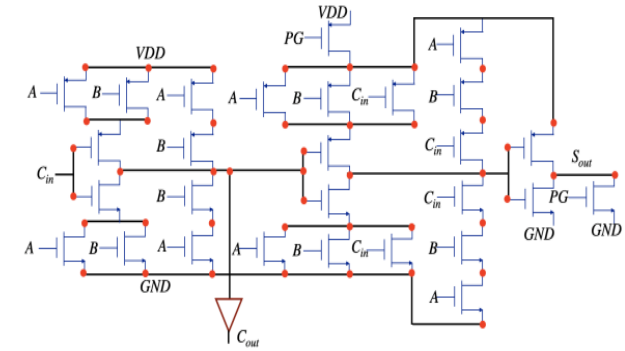

Figure 2: Circuit diagram of SESA2 adder

As a result of this, SESA2 adder has errors in SUM bits for input combinations 001, 010, 100, and 111. The CARRY output remains same irrespective of whether SESA2 adder operates in exact or approximate mode. In exact mode, the SUM output is computed using the normal SUM module. In approximate mode, the SUM module is PG and the approximate output which is equal to 0 is generated using a PG-controlled NMOS that pulls down the SUM output to a 0 as shown in Figure.

2.3 SESA3 ADDER

In SESA3 adder, we introduce approximation in the SUM output by making it 1 for all the input combinations as shown in Table II. As a result of this, SESA3 adder has errors in SUM bits for input combinations 000, 011, 101, and 110. The CARRY output remains same irrespective of whether SESA3 adder operates in exact or approximate mode. In exact mode, the SUM output is computed using the normal SUM module. In approximate mode, the SUM module is PG and the approximate output which is equal to 1 is generated using a PG-controlled NMOS that pulls down the complement of SUM to a permanent 0. Since this is connected to an inverter, we get the SUM output in approximate mode to be a 1 as shown in Figure.

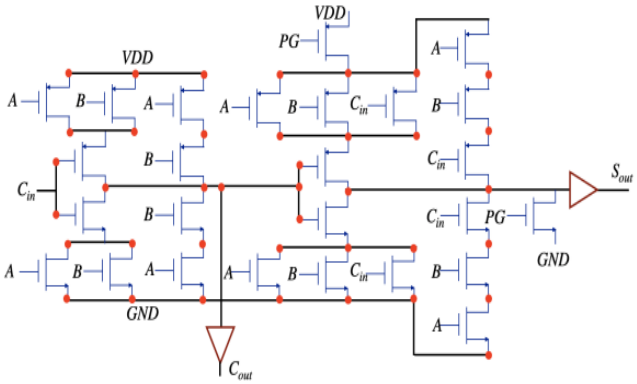

Figure 3: Circuit diagram of SESA3 adder

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3. PROPOSED WORK

3.1 SEDA ADDER

The SEDA adders surpasses the SESA adder in terms of advancement. Additionally, it possesses a maximum limit on the potential inaccuracy and offers the possibility to be customized. In contrast to SESA adders, which are limited to performing only one approximate addition, SEDA adders have the capability to do two approximate additions when operating in approximation mode. In the framework of SESA, we implement power gating for the SUM module of the adder, particularly when it is used in approximation mode. This is done in order to ensure safety and efficiency. Additionally, the SUM module is utilized within the SEDA adder in order to generate an extra CARRY.

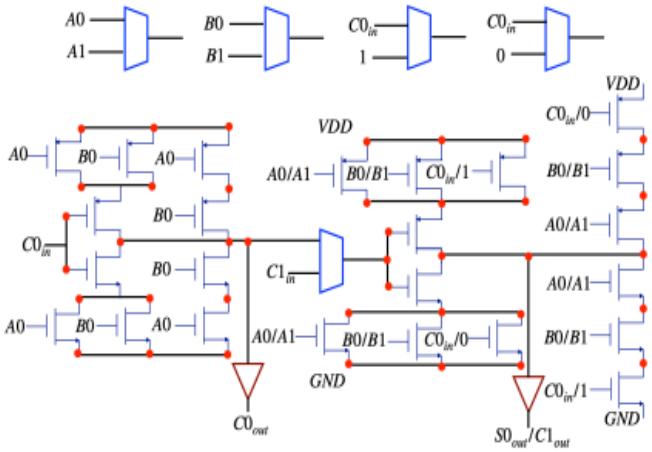

Figure 4: Circuit diagram of SEDA adder

3.2 8-Bit Approximate Multiplier

The number of stages of the proposed multiplier is one stage less than that of the former. At the last stage of the proposed multiplier, in order to obtain the summation of the three remaining rows of partial product, an especial CPA is used which was constructed by some half adders and some proposed approximate compressors. In each of the columns 2 and 15 of this CPA, a half adder is used, and in each of the columns 3 to 14, the first proposed compressor is used. Indeed, columns 3-14 of this CPA is our proposed CPA introduced in the previous sub-section which does not have the carry propagate delay problem

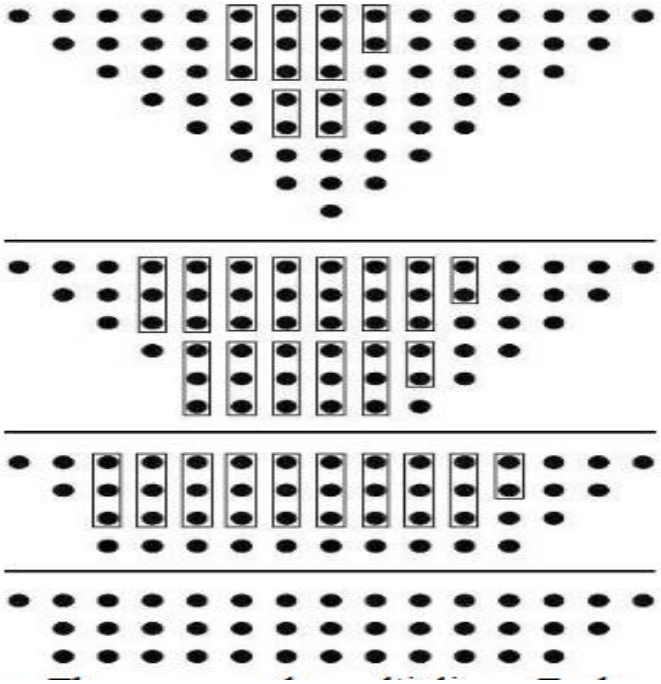

Figure 6: Approximate Multiplier

The proposed multiplier shown each rectangle represents a half adder or a full adder. Sum of the last stage's columns are computed using a CPA which is constructed by some half adders, full-adders, and proposed 4:2 compressors.

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4. SIMULATION RESULTS

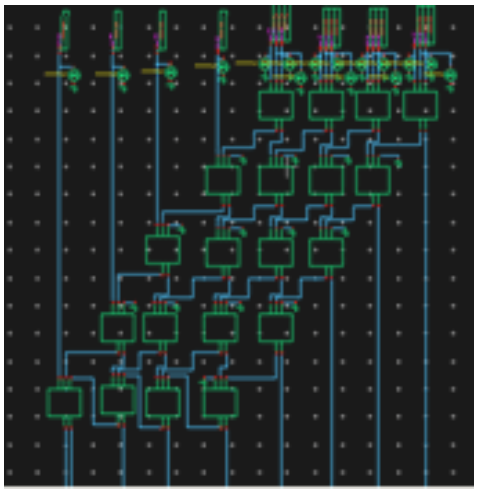

Figure 7: Approximate Multiplier using 4:2 Compressor

5. CONCLUSION

The design of a 4:2 compressor using single exact single approximate adders and single exact dual approximate adders has demonstrated the potential of approximate computing in achieving improved power efficiency and area reduction with minimal accuracy trade-offs. The approach leverages the concept of approximate adders to optimize the compressor design, making it suitable for applications where absolute precision is less critical. Approximate adders minimize the number of switching events and reduce overall capacitance, resulting in lower dynamic power requirements. This makes the design highly suitable for power-sensitive applications, such as embedded systems and IoT devices. The design shows a marked reduction in transistor count and layout area compared to traditional exact-only designs. Using approximate adders reduces the number of required logic elements, allowing for a more compact layout that is advantageous in high-density integrated circuits. The simplified logic in approximate adders contributes to reduced propagation delay, enhancing the overall speed of the compressor. This speed improvement makes the design appropriate for high-speed applications where minor accuracy trade-offs are acceptable, such as image and signal processing.

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